矽统科技

HY17P41
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded High Resolution 24-Bit ΣΔADC

Table of Contents

注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.sis.com。

2、 本規格書中的圖形、應用電路等，因第三方工業所有權引發的問題，本公司不承擔其責任。

3、 本產品在單獨應用的情況下，本公司保證它的性能、典型應用和功能符合說明書中的條件。當使用在客戶的產品或設備中，以上條件我們不作保證，建議客戶做充分的評估和測試。

4、 請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

5、 本產品雖內置防靜電保護電路，但請不要施加超過保護電路性能的過大靜電。

6、 本規格書中的產品，未經書面許可，不可使用在要求高可靠性的電路中。例如健康醫療器械、防災器械、車輛器械、車載器械及航空器械等對人體產生影響的器械或裝置，不得作為其部件使用。

7、 本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計並採用安全指標，這樣可以避免事故的發生。

8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- **8-Bit RISC-like 微控制器**
  - 8 位元加強型精簡指令 H08E CPU core，具有 61 條高性能指令集
  - 支援 C 語言開發環境
  - Power On & Brown Out Reset
  - WDT(Watch dog Timer)
- **工作電壓與操作溫度範圍**
  - VDD：2.0V ~ 5.5V 數位工作電壓
  - 2.4V ~ 5.5V 類比工作電壓
  - - 40°C ~ 85°C 工作溫度
- **記憶體**
  - 4kW OTP type 程式記憶體
  - 256 bytes SRAM 資料記憶體
  - 64 words Built-In EPROM(BIE)資料記憶
  - 6 層堆疊
- **低功耗特性**
  - 運行模式：250uA@3.0V、3.686MHz/2
  - 休眠模式：1.1uA@3.0V、14.5KHz
  - 待機模式：0.4uA@3.0V、all clock stop
- **工作頻率**
  - 內置高精度 RC 震盪器，有多種 CPU 工作時脈切換選擇，以達到最佳省電應用
  - 內置高速HAO震盪器,共有三種頻率可選：2.15MHz、4.147MHz、8.755MHz
  - 內置低功耗 LPO 震盪器 14.5KHz
- **多個可編程複用型 I/O**
  - 最多支援 7 支通用型數位輸出入腳，而該腳也同時具備不同的複用功能
- **24-Bit ΣΔADC 類比數位轉換器**
  - 最高取樣頻率達 921KHz
  - 超取樣頻率設置 64 ~ 32768
  - 二/三階梳狀濾波器，轉換頻率 15.6Ksps
  - 有 1/4 ~ 32 倍輸入端信號放大倍率可選擇
  - 有 1/2 ~ 1 倍參考端信號放大倍率可選擇
  - 全差動輸入信號與測量範圍的零點調整
  - 低溫飄係數與內置絕對溫度傳感器
- **REFO 穩壓電壓源**
  - 可供傳感器驅動使用(驅動能力 5mA max.)
  - 可設置穩壓輸出：1.2V/2.0V/2.4V/3.0V
  - 採可外灌輸入電壓設計
- **LVD 低電壓檢測功能具 4 段檢測電壓設置與外部輸入電壓檢測功能**
- **通訊介面**
  - I^2C(Master & Slave) 通訊介面
  - EUART 通訊介面
  - 單電源架構設計，2 線式 ICP 燒錄引腳即可滿足 OTP 燒錄
- **計時器**
  - Watch Dog
  - 8-bit Timer A
  - 16-bit Timer B
    - ◆ 1ch 16-Bit PWM or 2ch 8-bit PWM
- **封裝**
  - MSOP10、DFN8、SOP8、SOT23-6
- **應用領域**
  - 壓阻式電橋感測器
  - PIR 感測器、數位 PIR 感測器

功能列表

Model No.	VDD (V)	Internal Clock (Hz)	System Clock (Hz)	Program Memory (word)	SRAM (byte)	BIE (word)	ADC ENOB (bit x ch)	Sample Rate (sps)	I/O	Timer (bit x ch)	PWM (bit x ch)	Serial Interface (I/F x ch)	Package
HY17P41	2.0~5.5	14.5K 2.15M 4.147M 8.755M	14.5K~8M	4K	256	64	19-bit x 4	31~15.6K	4xIO	8-bit x 1 16-bit x 1	8-bit x 2 16-bit x 1	EUART x 1 I^2C x 1	SOT23-6
							19-bit x 6		6xIO				DFN8 SOP8
							19-bit x 7		7xIO				MSOP10

2. 引腳定義

2.1. MSOP10 引腳圖

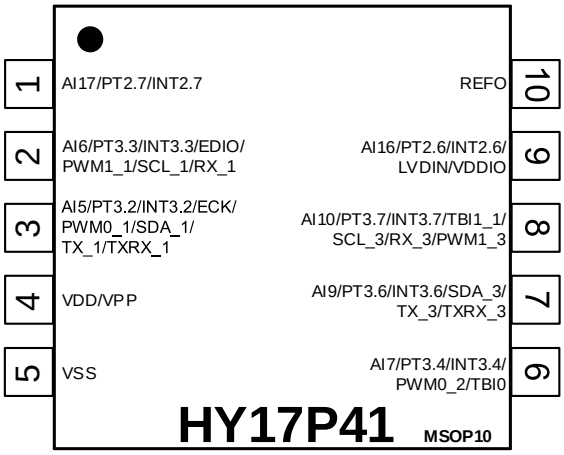


圖 2-1 MSOP10 引腳圖

2.2. DFN8 引腳圖

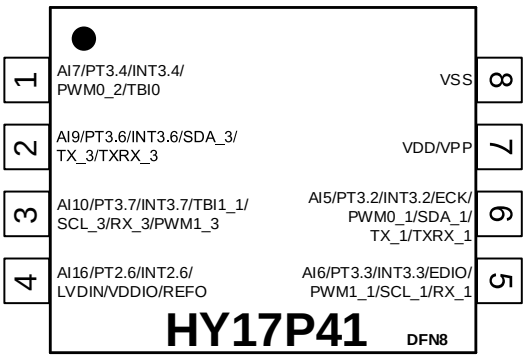


圖 2-2 DFN8 引腳圖

2.3. SOP8 引腳圖

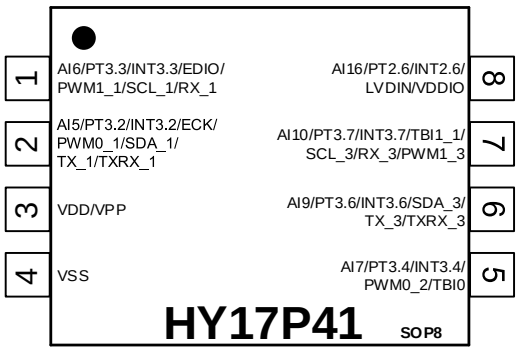


圖 2-3 SOP8 引腳圖

2.4. SOT23-6 引腳圖

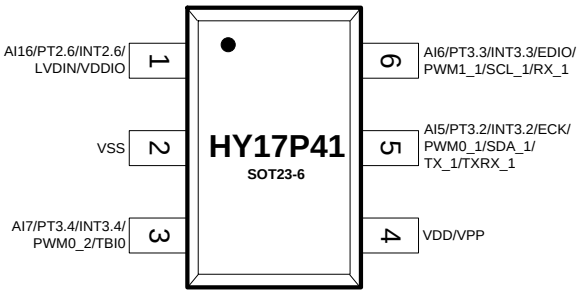


圖 2-4 SOT23-6 引腳圖

2.5. I/O 定義與說明

"I/O"輸入/輸出,"I"輸入,"O"輸出,"S"史密斯觸發,"C"CMOS 特性兼容輸出與輸入,"P"電壓源,"A"類比通道

引腳編號				引腳名稱	引腳特性		功能說明
MSOP10	DFN8	SOP8	SOT23-6		格式	緩衝	
4	7	3	4	VDD/VPP			
				VDD	P	P	工作電壓源，需外接 1~10uF 至 VSS
				VPP	P	P	OTP 燒寫的電壓源輸入引腳
5	8	4	2	VSS	P	P	晶片工作電壓源接地端
10	4	-	-	REFO	P	P	穩壓電壓源，可供傳感器驅動電源（依需求來外接穩壓電容）
9		8	1	AI16/PT2.6/INT2.6/LVDIN/VDDIO			
				AI16	A	A	類比輸入通道 16
				PT2.6	I/O	S/C	數位輸入/輸出引腳
				INT2.6	I	S	外部中斷源輸入引腳
				LVDIN	A	A	低電壓偵測外部信號輸入引腳
				VDDIO	P	P	PT3.2/3.3/3.6/3.7 電源輸入引腳
1	-	-	-	AI17/PT2.7/INT2.7			
				AI17	A	A	類比輸入通道 17
				PT2.7	I/O	S/C	數位輸入/輸出引腳
				INT2.7	I	S	外部中斷源輸入引腳
7	2	6	-	AI9/PT3.6/INT3.6/SDA_3/TX_3/ TXRX_3			
				AI9	A	A	類比輸入通道 9
				PT3.6	I/O	S/C	數位輸入/輸出引腳
				INT3.6	I	S	外部中斷源輸入引腳
				SDA_3	I/O	S/C	I²Cs 通訊數據信號引腳
				TX_3	O	C	EUART 通訊傳送信號接口
				TXRX_3	I/O	S/C	EUART 單線雙向通訊介面接口 (外部需要連接上拉電阻)
8	3	7	-	AI10/PT3.7/INT3.7/TBI1_1/SCL_3/ RX_3/PWM1_3			
				AI10	A	A	類比輸入通道 10
				PT3.7	I/O	S/C	數位輸入/輸出引腳
				INT3.7	I	S	外部中斷源輸入引腳
				TBI1_1	I	S	Timer B CPI 輸入選擇源

				SCL_3	I/O	S/C	I²Cs 通訊時鐘信號引腳
				RX_3	I	S	EUART 通訊接收信號接口
				PWM1_3	O	C	PWM1 輸出引腳
3	6	2	5	AI5/PT3.2/INT3.2/ECK/PWM0_1/ SDA_1/TX_1/TXRX_1			
				AI5	A	A	類比輸入通道 5
				PT3.2	I/O	S/C	數位輸入/輸出引腳
				INT3.2	I	S	外部中斷源輸入引腳
				ECK	I	S	ICP 通訊時脈信號
				PWM0_1	O	C	PWM0 輸出
				SDA_1	I/O	S/C	I²Cs 通訊數據信號引腳
				TX_1	O	C	EUART 通訊傳送信號接口
				TXRX_1	I/O	S/C	EUART 單線雙向通訊介面接口 (外部需要連接上拉電阻)
2	5	1	6	AI6/PT3.3/INT3.3/EDIO/PWM1_1/ SCL_1/RX_1			
				AI6	A	A	類比輸入通道 6
				PT3.3	I/O	S/C	數位輸入/輸出引腳
				INT3.3	I	S	外部中斷源輸入引腳
				EDIO	I/O	S/C	ICP 通訊數據信號引腳
				PWM1_1	O	C	PWM1 輸出
				SCL_1	I/O	S/C	I²Cs 通訊時脈信號引腳
				RX_1	I	S	EUART 通訊接收信號接口
6	1	5	3	AI7/PT3.4/INT3.4/PWM0_2/TBI0/LVDO			
				AI7	A	A	類比輸入通道 7
				PT3.4	I/O	S/C	數位輸入/輸出引腳
				INT3.4	I	S	外部中斷源輸入引腳
				PWM0_2	O	C	PWM0 輸出
				TBI0	I	S	Timer B CPI 輸入選擇源

表 2-1 引腳編號與說明

2.6. 復用引腳定義說明

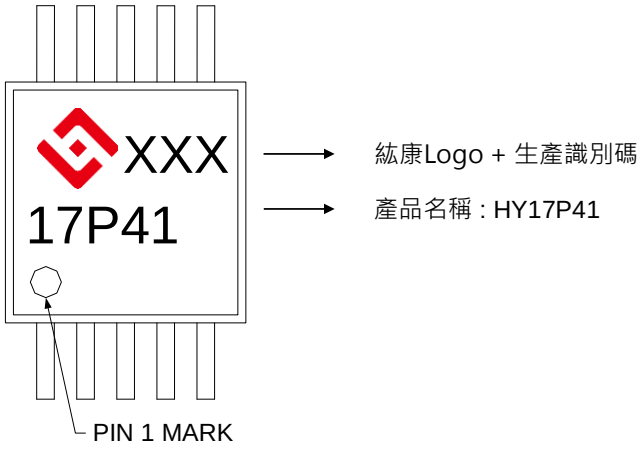
Function	I/O Type	Interrupt	Internal Pull high	ICP	Timer B Enable	I²C	UART	Special	Analog	PWM
PT2.6	DAI/O	INT2.6	PU2.6					LVDIN VDDIO	AI16	
PT2.7	DAI/O	INT2.7	PU2.7						AI17	
PT3.6	DAI/O	INT3.6	PU3.6			SDA_3	TX_3		AI9	
PT3.7	DAI/O	INT3.7	PU3.7		TBI1_1	SCL_3	RX_3		AI10	PWM1_3
PT3.2	DAI/O	INT3.2	PU3.2	ECK		SDA_1	TX_1		AI5	PWM0_1
PT3.3	DAI/O	INT3.3	PU3.3	EDIO		SCL_1	RX_1		AI6	PWM1_1
PT3.4	DAI/O	INT3.4	PU3.4		TBI0				AI7	PWM0_2

表 2-1 引腳編號與說明

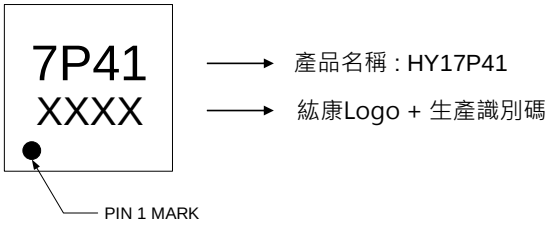
Note：複用腳不管是輸入或是輸出的複用功能，默認的狀態都是關閉。

2.7. 封裝片標記信息

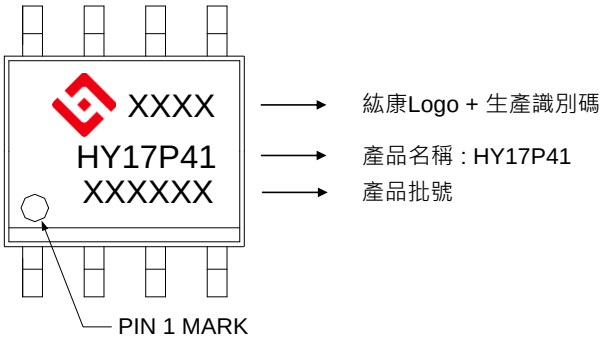
2.7.1. MSOP10 封裝片標記信息



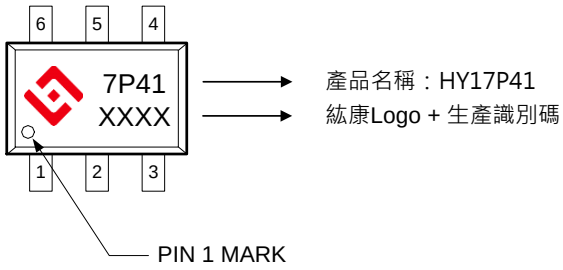
2.7.2. DFN8 封裝片標記信息



2.7.3. SOP8 封裝片標記信息



2.7.4. SOT23-6 封裝片標記信息



3. 應用電路

3.1. 數位壓力感測器應用

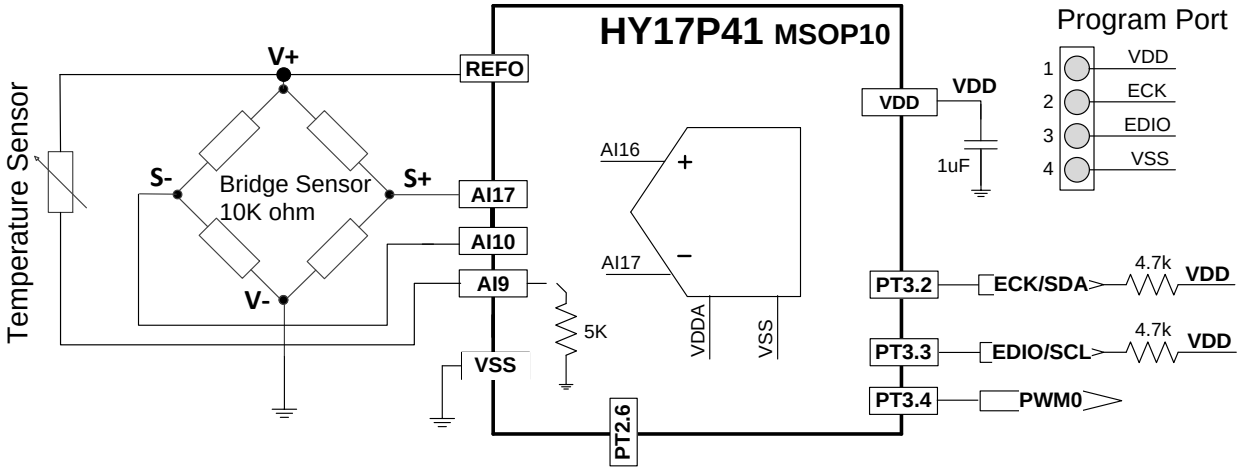


圖 3-1 數位壓力感測器應用參考電路

3.2. PIR 感測器應用

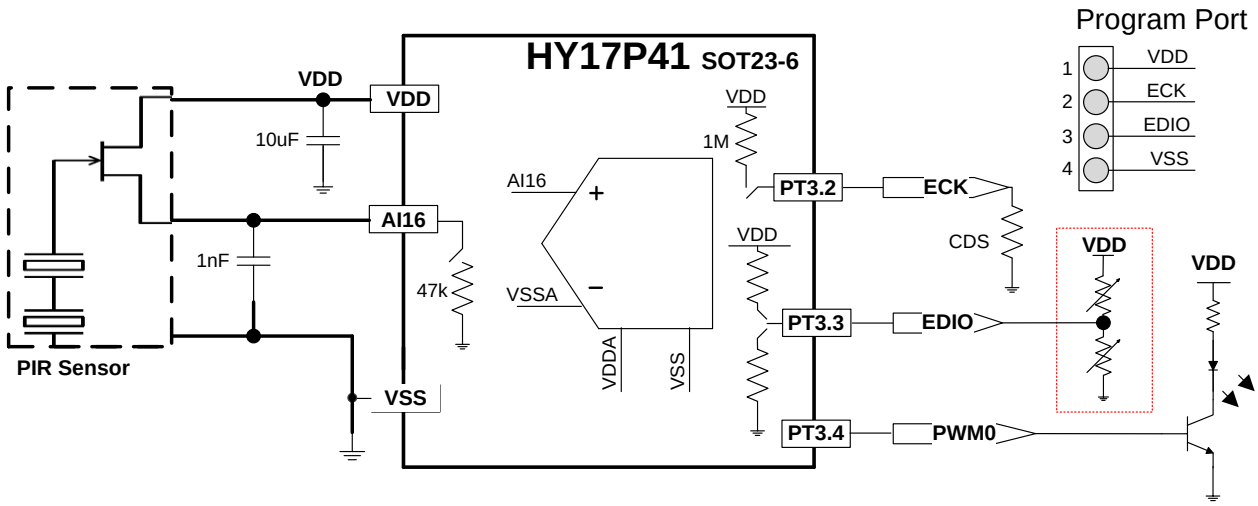


圖 3-2 PIR 感測器應用參考電路

3.3. 數位 PIR 感測器應用

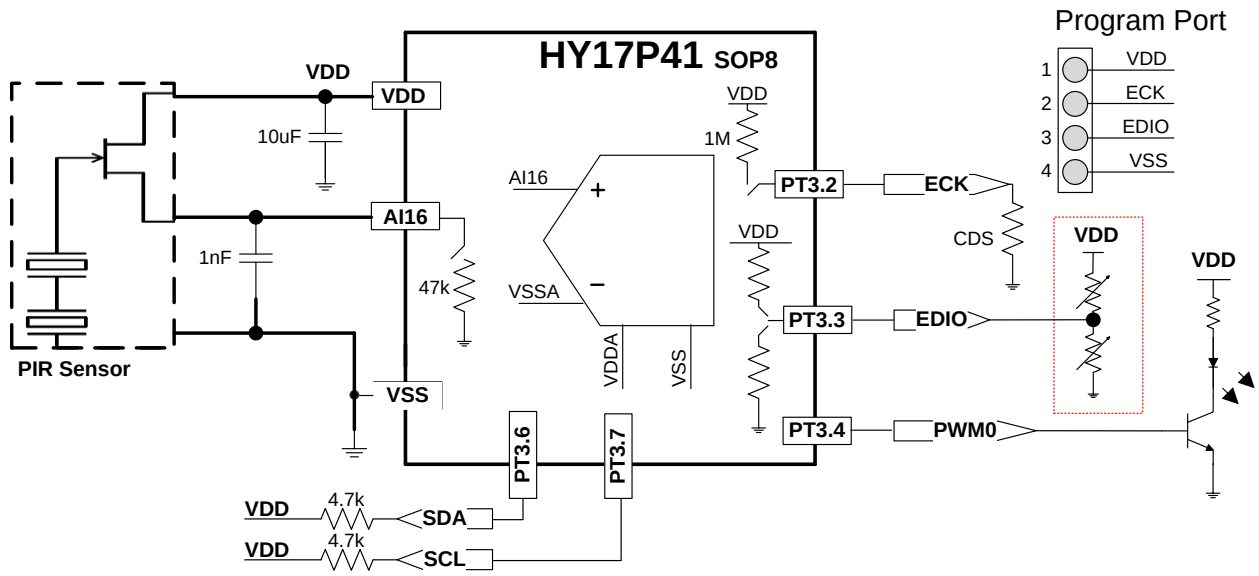


圖 3-3 數位 PIR 感測器應用參考電路

3.4. 應用電路注意事項

● PIR 感測器應用電路：

可以支援外部電阻調整 PIR Sensitivity and LED On Time 參數；如果可以使用 Writer 將參數燒錄於 BIE 區域，則應用電路紅框中的分壓電阻可以省略，只需 5PIN 即可滿足 PIR 偵測 + CDS 感光偵測 + PWM 輸出。

● OTP 晶片燒錄：

由於 VDD 與 VPP(OTP 燒錄的 8V 電壓源輸入引腳)是共腳，所以為了避免 OTP 在燒錄過程 VPP 的 8V 高壓損壞 IC 周邊的元件，故建議不要在板上燒錄 OTP 晶片，請單獨燒好 OTP 封裝片後再上板；如果一定要在板上做燒錄，可先在晶片 VDD/VPP 腳至周邊的路徑預留短路焊點，待上板燒錄 OTP 晶片動作完成後再短路。

● REFO 傳感器驅動電源：

REFO 電壓源可用來做為傳感器的驅動電源，可由晶片內部設置輸出電壓 (共有 4 段電壓 1.2V/2.0V/2.4V/3.0V 可選擇)或是由外灌輸入電壓；當採晶片內部設置輸出電壓源時要注意，該源驅動能力最大只有 5mA，在應用時須依需求外接 0~100uF 的對地電容。

4. Function Outline

4.1. 內部方塊圖

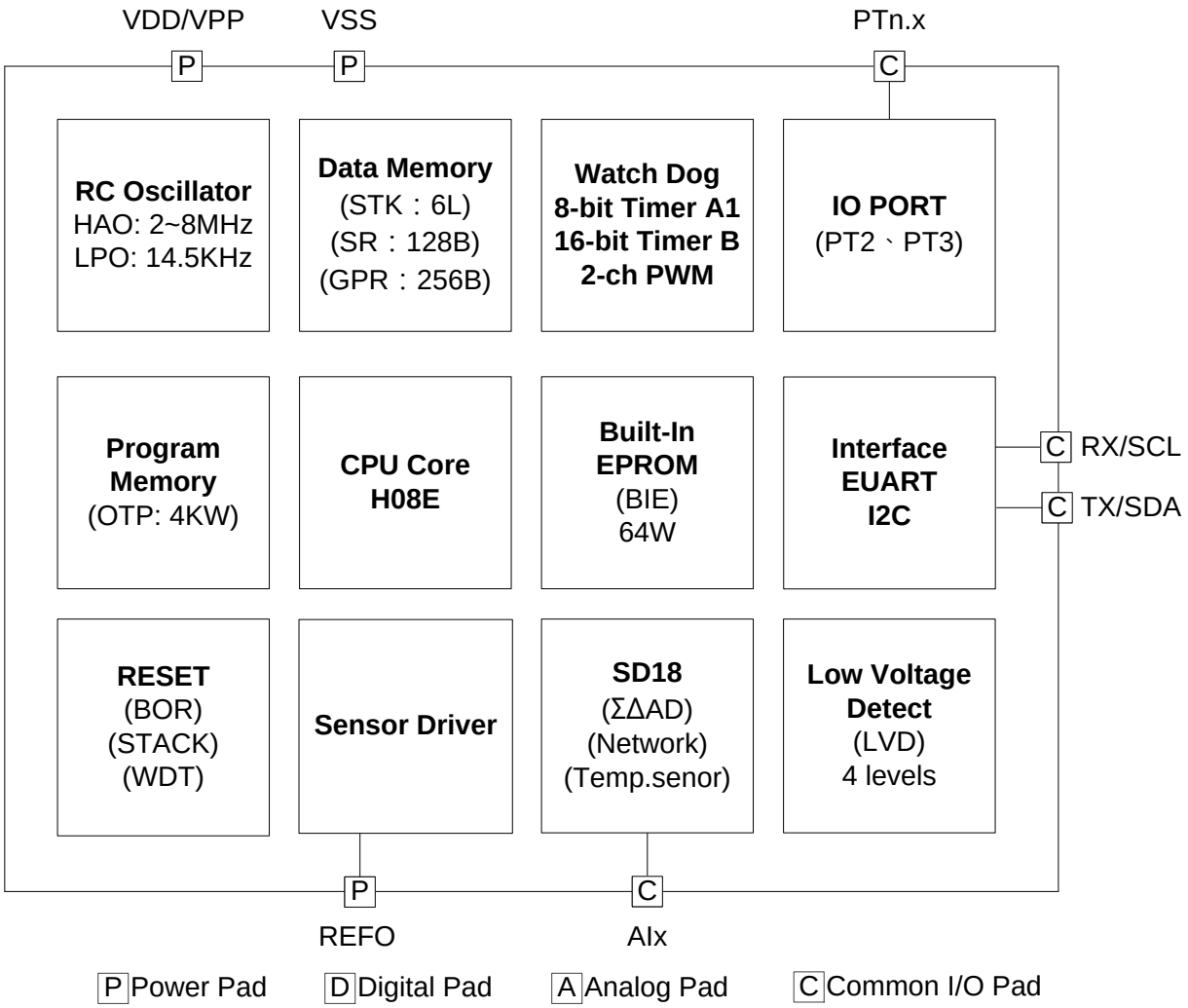


圖 4-1 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY17P41	HY17P41 規格說明書
UG-HY17P41	HY17P41 使用說明書
APD-CORE002	H08A、H08C、H08D 組合語言指令集說明書

開發工具相關使用說明書

APD-HY17MIDE001	HY17M Series Assembly IDE 軟體使用說明書
APD-HYIDE016	H08 CIDE 軟體使用說明書
APD-HY17MIDE010	HY17M26 Series IDE 硬體使用說明書

產品生產相關使用說明書

APD-HYIDE020	HY10000-WK09 整合型燒錄器使用說明書

4.3. Clock System

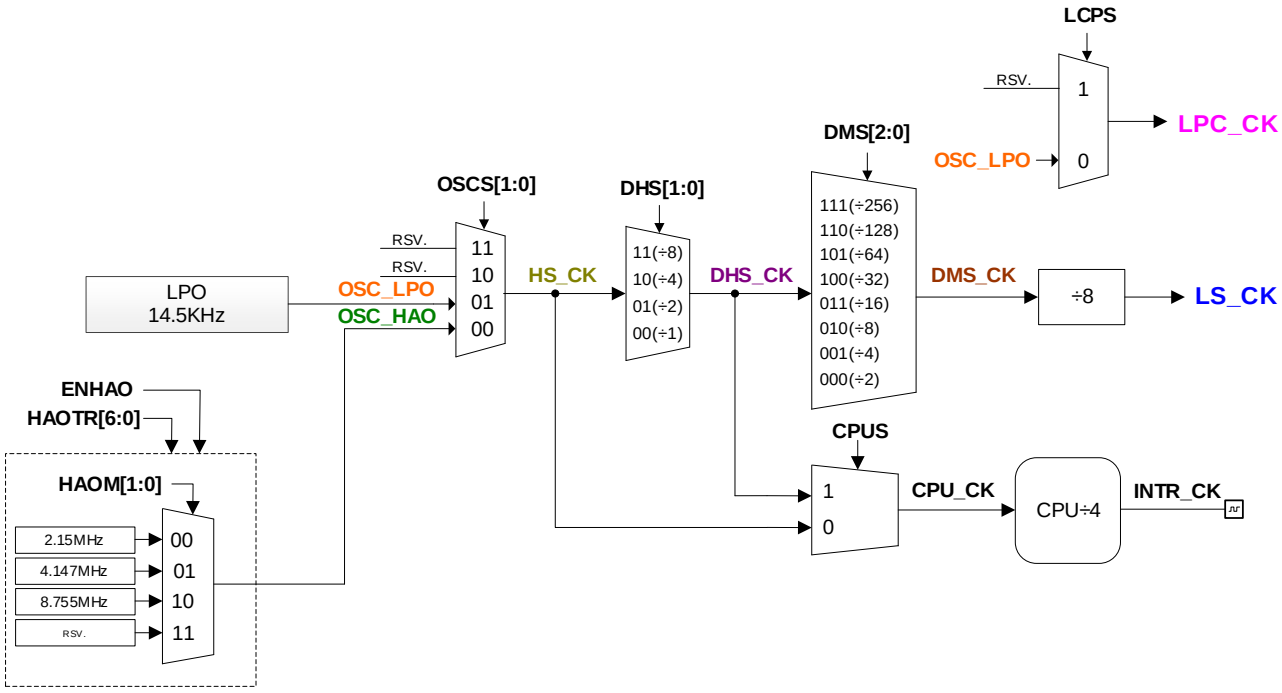


圖 4-2 Clock System(一) 方塊圖

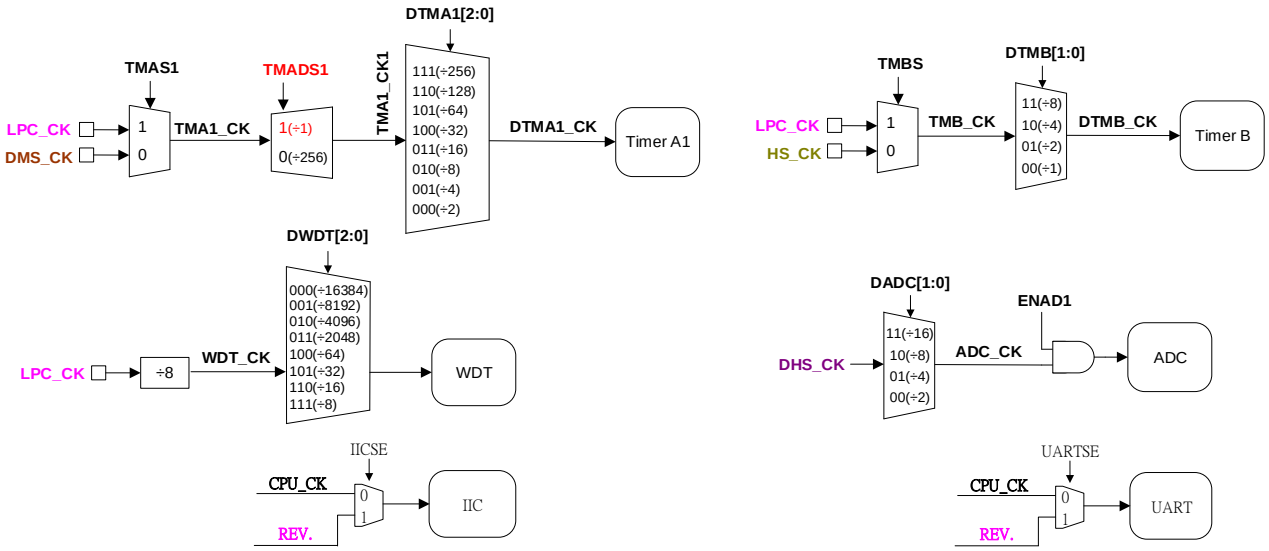


圖 4-3 Clock System(二) 方塊圖

4.4. GPIO PT2~ PT3 System

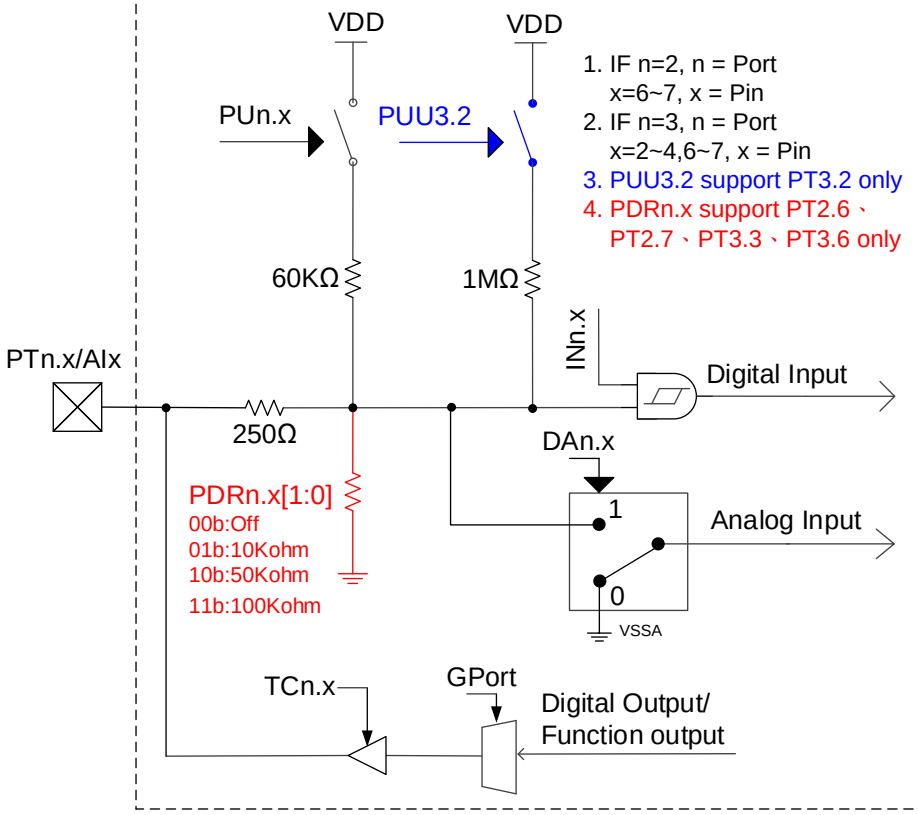


圖 4-4 GPIO PT2~ PT3 System 方塊圖

4.5. Reset System

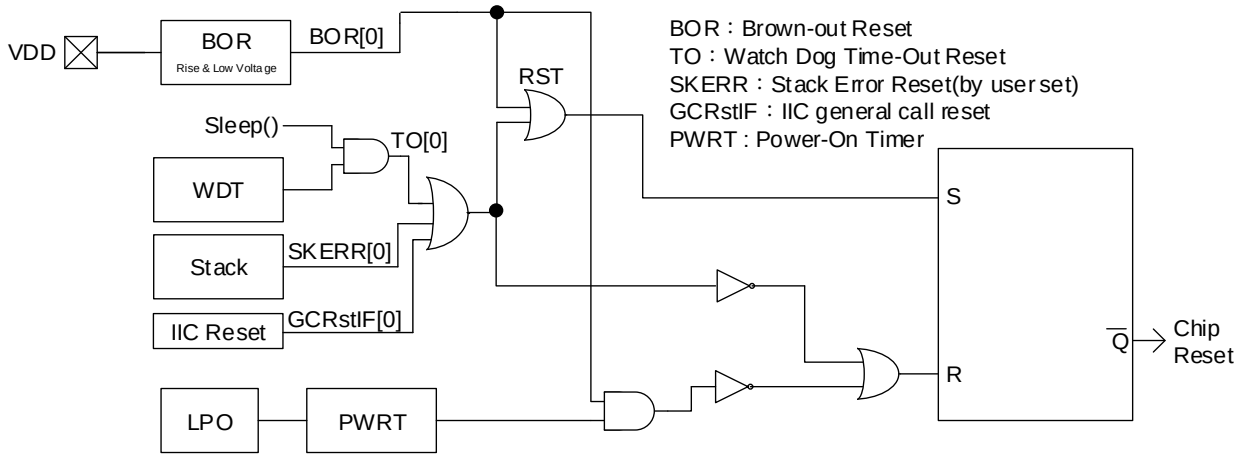


圖 4-5 Reset System 方塊圖

4.6. Power System

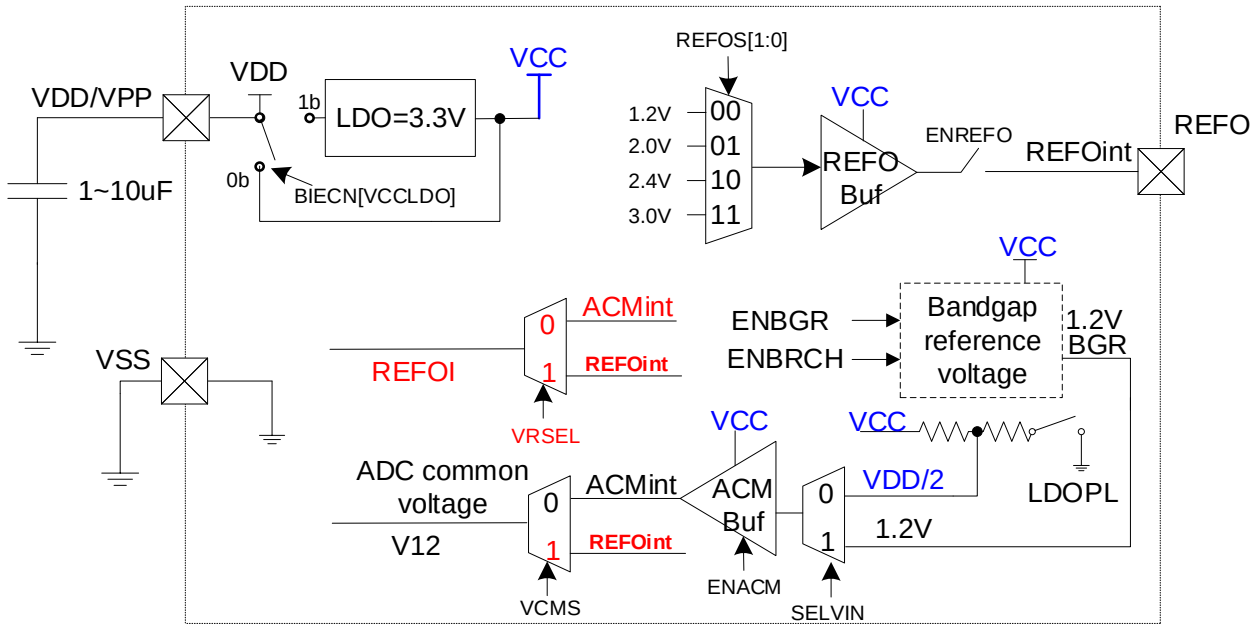
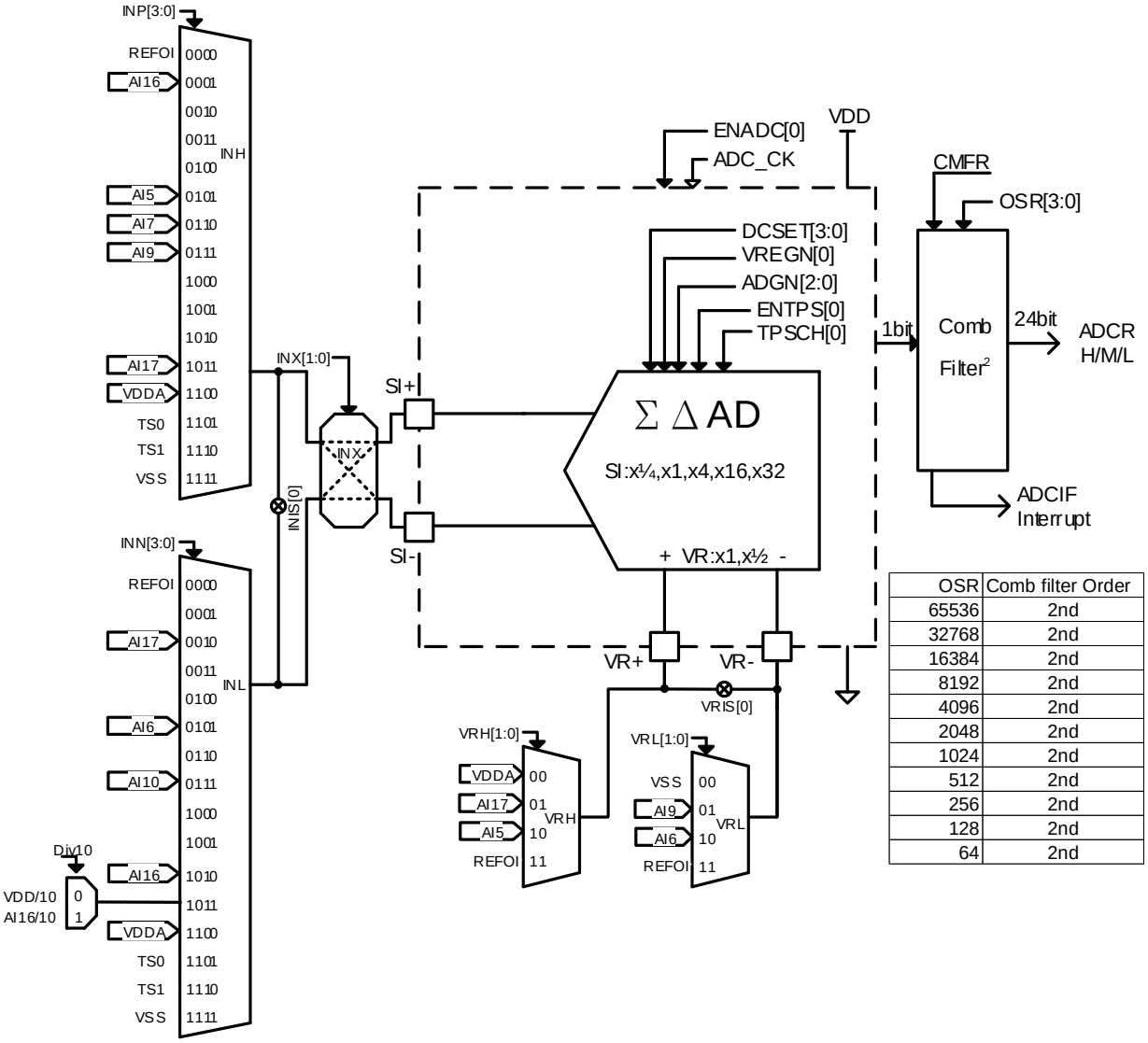


圖 4-6 Power System 方塊圖

4.7. ADC Network System



OSR	Comb filter Order
65536	2nd
32768	2nd
16384	2nd
8192	2nd
4096	2nd
2048	2nd
1024	2nd
512	2nd
256	2nd
128	2nd
64	2nd

圖 4-7 ADC Network System 方塊圖

4.8. Low Voltage Detect(LVD) System

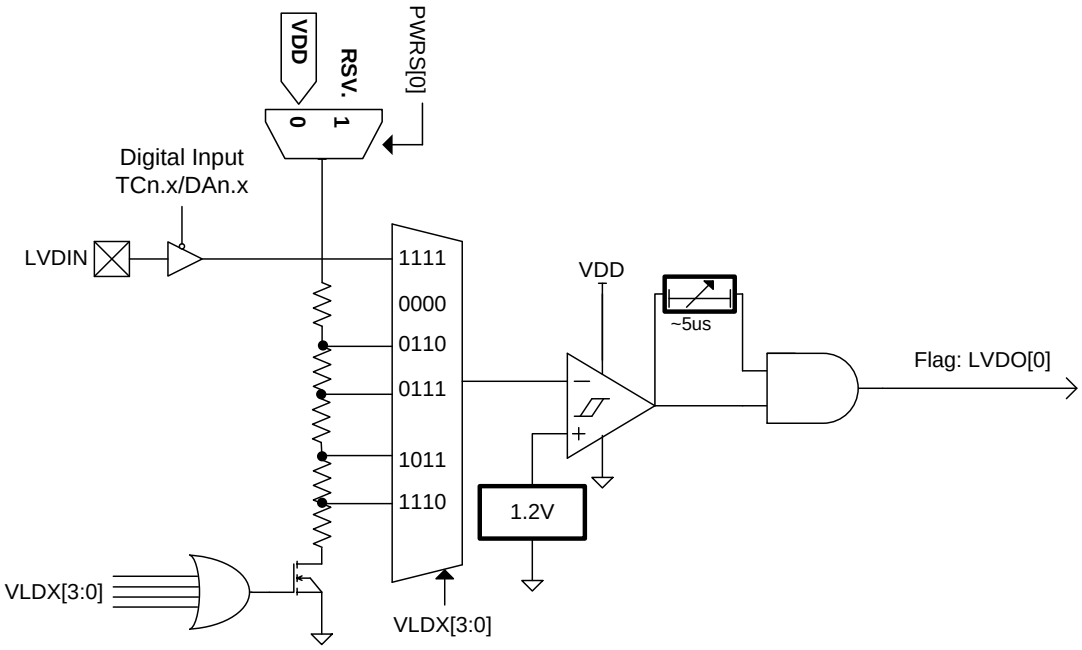
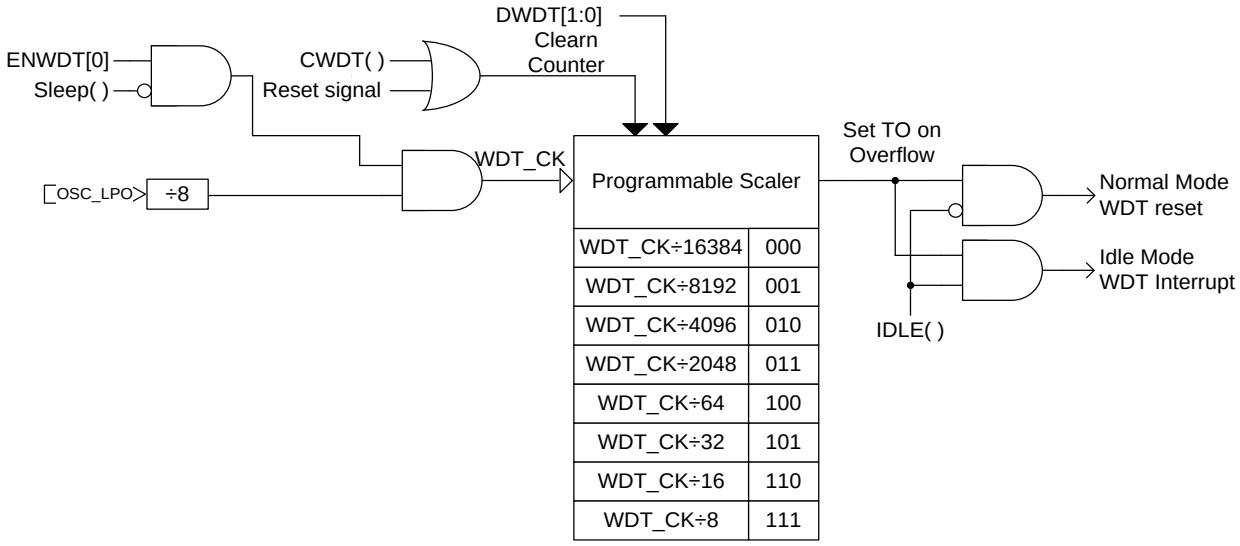


圖 4-8 Low Voltage Detect System 方塊圖

4.9. Watch Dog System



WDT_CK÷16384	000
WDT_CK÷8192	001
WDT_CK÷4096	010
WDT_CK÷2048	011
WDT_CK÷64	100
WDT_CK÷32	101
WDT_CK÷16	110
WDT_CK÷8	111

圖 4-9 Watch Dog System 方塊圖

4.10. 8-bit Timer A1 (TMA1) System

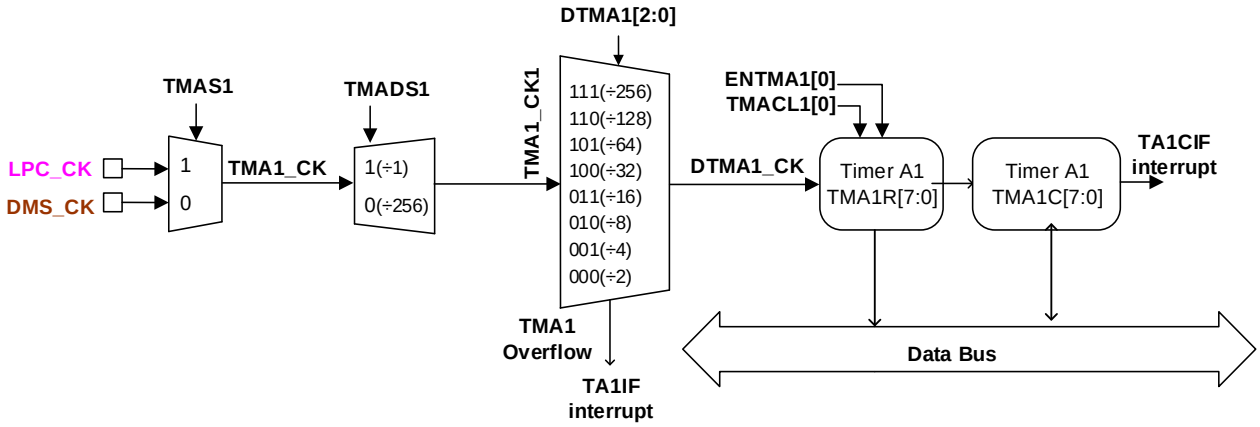


圖 4-10 8-bit Timer A1 (TMA1) System 方塊圖

4.11. 16-bit Timer B (TMB) System

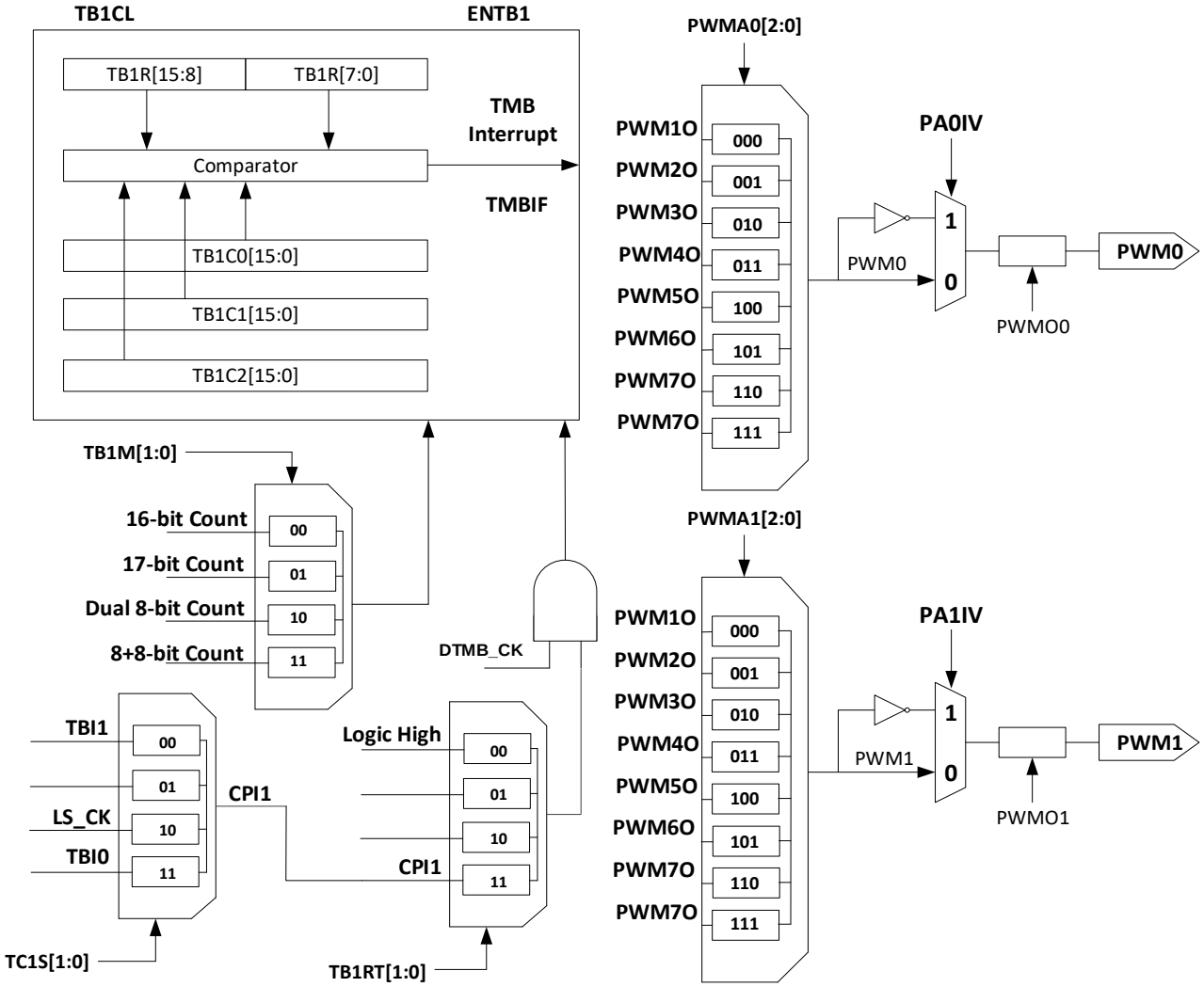


圖 4-11 16-bit Timer B (TMB) System 方塊圖

4.12. I²C System

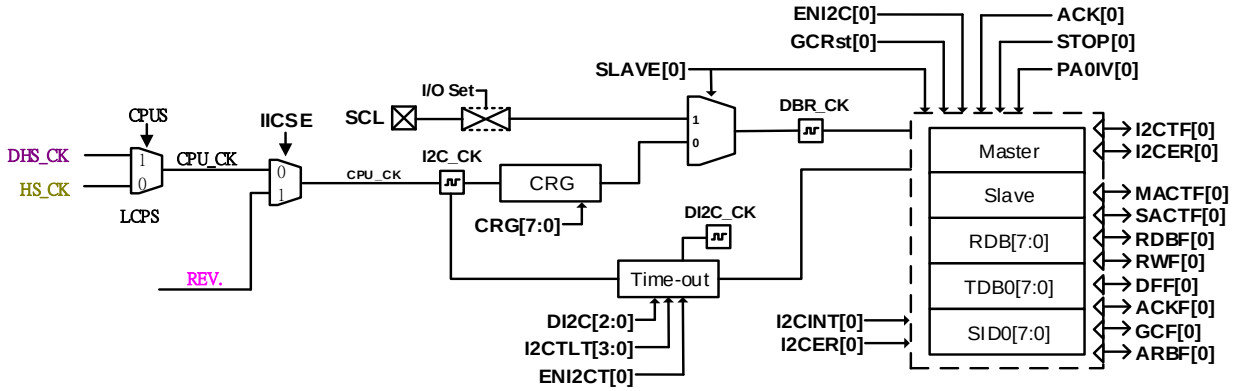


圖 4-12 I²C System 方塊圖

4.13. EUART System

EUART TRANSMIT BLOCK DIAGRAM

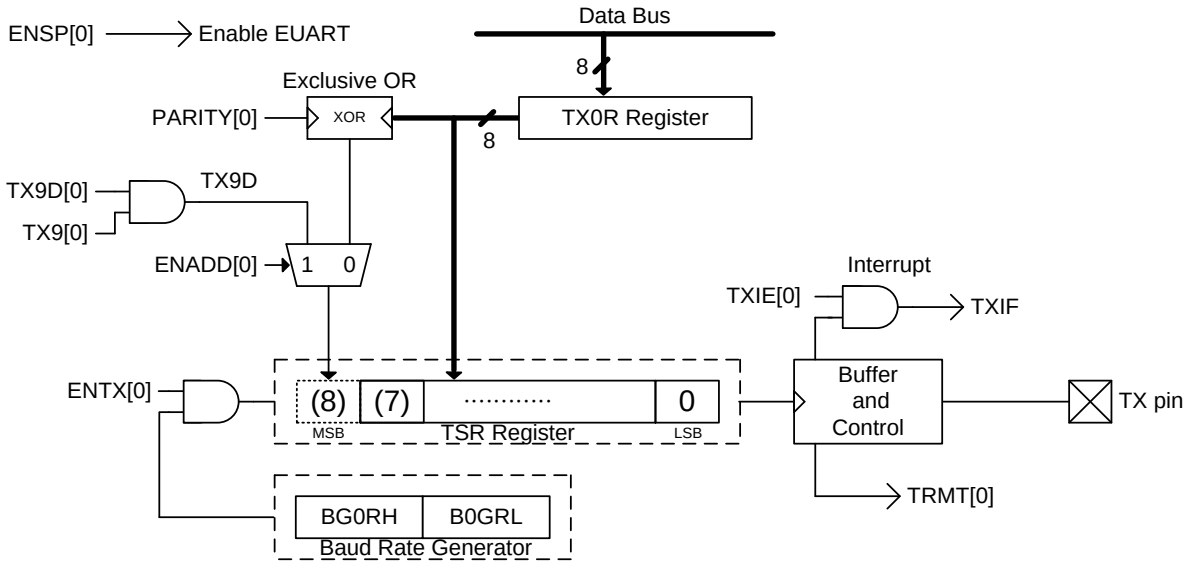
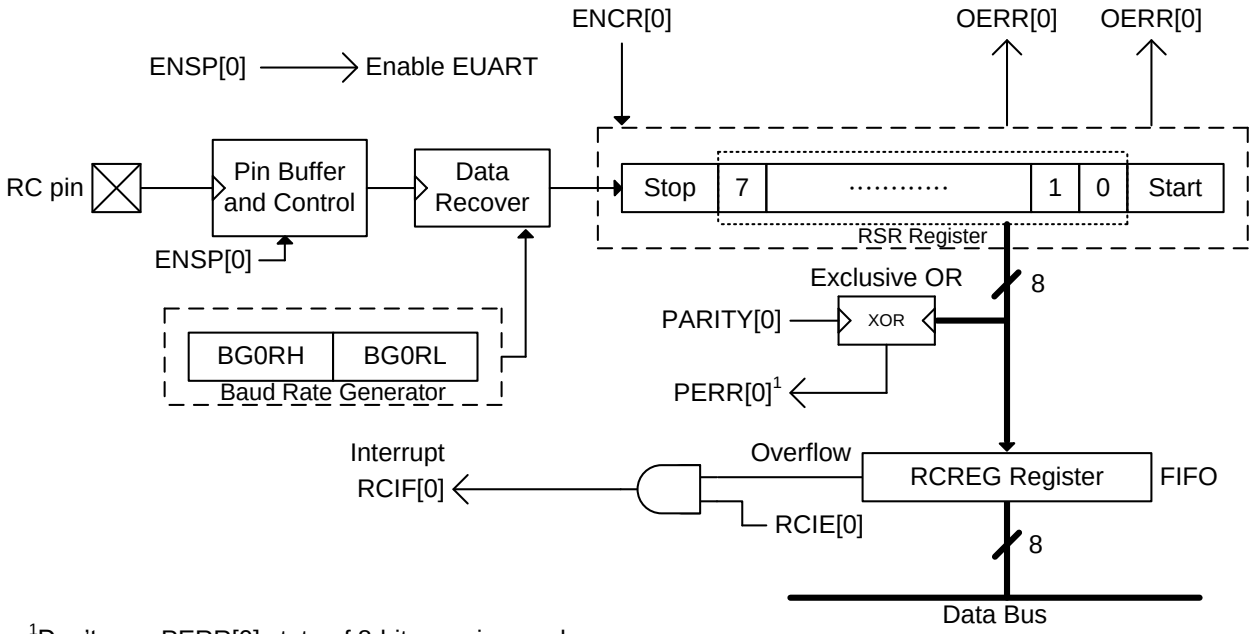


圖 4-13 EUART 傳送方塊圖

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

圖 4-14 EUART 8-bits 接收方塊圖

5. 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremente								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremente								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008h	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ah	INDF2	Contents of FSR2 to address data memoryvalue of FSR2 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Bh	POINC2	Contents of FSR2 to address data memoryvalue of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ch	PODEC2	Contents of FSR2 to address data memoryvalue of FSR2 post-decremente								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Dh	PRINC2	Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Eh	PLUSW2	Contents of FSR2 to address data memoryvalue of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Fh	FSR0H	-	-	-	-	-	-	-	FSR0[8]	x	....u	-,-,-,- -,-,-,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR1H	-	-	-	-	-	-	-	FSR1[8]	x	....u	-,-,-,- -,-,-,*
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
013h	FSR2H	-	-	-	-	-	-	-	FSR2[8]	x	....u	-,-,-,- -,-,-,*
014h	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	-	TOS[11:8]				 xxxx	.... uuuu	-,-,-,- *,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	SKPRT[3:0]				000. 0000	u$$. $$$$	rw0,rw0,rw0,- *,*,*,*
01Ah	PCLATH	-	-	-	-	PC[11:8]				 0000	 0000	-,-,-,- *,*,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Dh	TBLPTRH	-	-	-	-	TBLPTR11:8]				 xxxx	.... uuuu	-,-,-,- *,*,*,*
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE	-	-	-	0000 0000	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	TA1IE	-	TXIE	RCIE	I2CERIE	I2CIE	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF	-	-	-	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	TA1IF	-	TXIF	RCIF	I2CERIF	I2CIF	-	-	0000 0000	uuuu uuuu	*,*,*,* r,r,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Ah	BSRCN	-	-	-	-	-	-	-	BSR[0]	x	....u	-,-,-,- -,-,-,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
02Ch	PSTAT	BOR	PD	TO	IDL	-	SKERR	-	GCRstIF	$000 .0.0	uu$u .$.u	rw0,rw0,rw0,rw0 -,rw0,-,rw0
030h	PWRCN	ENBGR							CSFON	1000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
031h	OSCCN0	-	OSCS[0]	DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
032h	OSCCN1	CCOPT	-	DADC[1:0]		DTMB[1:0]		TMBS	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
033h	OSCCN2	IDLEM1	IDLEM0	-	-	-	HAOM[1:0]		ENHAO	0000 0001	uuuu uuu1	*,*,*,*,*,*,*,*
035h	CSFCN0	SKRST	HAOTR[6:0]							.1..	uuuu uuuu	*,*,*,*,*,*,*,*
036h	CSFCN1	-	-	-	-	-	-	-	-	....	....	-,-,-,- -,-,-,-
038h	WDTCN	-	-	-	-	ENWDT	DWDT[2:0]			 0000	.... $000	-,-,-,- rw1,*,*,*
039h	AD1H	ADC1 conversion high byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
03Ah	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
03Bh	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
03Ch	AD1HH	-	-	-	-	-	-	-	-	....	....	-,-,-,- -,-,-,-
040h	AD1CN1	-	-	VREGN	REFOS[1:0]		ADGN[2:0]			xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
041h	AD1CN2	Div10	ENREFO	-	SELVIN	DCSET[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
042h	AD1CN3	INP[3:0]				INN[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
043h	AD1CN4	VRH[1:0]		VRL[1:0]		INX[1:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
044h	AD1CN5	ENACM	VRSEL	VCMS	LDOPL		TPSCP	ENTPS	TPSCH	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
045h	LVDCN	-	-	-	LVDS[3:0]				LVDO	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-1 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
045h	LVDCN	-	-	-	LVDS[3:0]				LVDO	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Bh	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-		0000 0000	u0uu uuuu	*,rw1,*,*,*,*,*,*
04Ch	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
04Dh	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
051h	TB1Flag		PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	.000 0000	.uuu uuuu	-,r,r,r r,r,r,r
052h	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	PWMO1	PWMO0	0000 0000	uuuu u0uu	*,*,*,*,*,rw1,*,*
053h	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
054h	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
055h	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
056h	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
057h	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
058h	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
059h	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
05Ah	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
05Bh	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
05Ch	TC1CN0	-	TC1S[1:0]		-	-	-	-	-	.00.	.uu.	-,*,*,- -,-,-,-
073h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,*,-,-,*
074h	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw0
075h	BA0CN	UARTSE	-	-	-	ENCR	RC9	ENADD	ENABD	 0000	.... uuuu	-,-,-,- *,*,*,*
076h	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
077h	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
078h	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
079h	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
180h	BIECN	ENBIE	BLKSEL	-	ENBVD	VPPHV	VCCLDO	BIEWR	BIERD	10.0 $000	10.0 $0uu	r1,*,-,* r,w1,*,*
181h	BIEARH	-	-	-	-	BIE Address Register as BIEAH[7:0]				xxxx xxxx	.... uuuu	r,-,-,- *,*,*,*
182h	BIEARL	BIE Address Register as BIEAL[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
183h	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
184h	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
185h	BIEKEY	BIE KEY Data Register								0000 0000	0000 0000	*,*,*,*,*,*,*,*
199h	PT2	PT2.7	PT2.6	-	-	-	-	-	-	xx..	xx..	*,*,-,- -,-,-,-
19Ah	PT2IN	IN2.7	IN2.6	-	-	-	-	-	-	00..	uu..	*,*,-,- -,-,-,-
19Bh	TRISC2	TC2.7	TC2.6	-	-	-	-	-	-	00..	uu..	*,*,-,- -,-,-,-
19Ch	PT2DA	DA2.7	DA2.6	-	-	-	-	-	-	00..	uu..	*,*,-,- -,-,-,-
19Dh	PT2PU	PU2.7	PU2.6	-	-	-	-	-	-	00..	uu..	*,*,-,- -,-,-,-
19Eh	PT2INT	INTG2.7	INTG2.6	-	-	-	-	-	-	00..	uu..	*,*,-,- -,-,-,-
19Fh	PT2INTE	INTE2.7	INTE2.6	-	-	-	-	-	-	00..	uu..	*,*,-,- -,-,-,-
1A0h	PT2INTF	INTF2.7	INTF2.6	-	-	-	-	-	-	00..	uu..	*,*,-,- -,-,-,-
1A1h	PT3	PT3.7	PT3.6	-	PT3.4	PT3.3	PT3.2	-	-	xx.x xx..	xx.x xx..	*,*,-,*,*,-,-
1A2h	PT3IN	IN3.7	IN3.6	-	IN3.4	IN3.3	IN3.2	-	-	00.0 00..	uu.u uu..	*,*,-,*,*,-,-
1A3h	TRISC3	TC3.7	TC3.6	-	TC3.4	TC3.3	TC3.2	-	-	00.0 00..	uu.u uu..	*,*,-,*,*,-,-
1A4h	PT3DA	DA3.7	DA3.6	-	DA3.4	DA3.3	DA3.2	-	-	00.0 00..	uu.u uu..	*,*,-,*,*,-,-
1A5h	PT3PU	PU3.7	PU3.6	-	PU3.4	PU3.3	PU3.2	-	-	00.0 00..	uu.u uu..	*,*,-,*,*,-,-
1A6h	PT3INT	INTG3.7	INTG3.6	-	INTG3.4	INTG3.3	INTG3.2	-	-	00.0 00..	uu.u uu..	*,*,-,*,*,-,-
1A7h	PT3INTE	INTE3.7	INTE3.6	-	INTE3.4	INTE3.3	INTE3.2	-	-	00.0 00..	uu.u uu..	*,*,-,*,*,-,-
1A8h	PT3INTF	INTF3.7	INTF3.6	-	INTF3.4	INTF3.3	INTF3.2	-	-	00.0 00..	uu.u uu..	*,*,-,*,*,-,-
1A9h	GPort0	-	-	GTBI1[2:0]			GTBI0[2:0]			..00 0000	..uu uuuu	-,-,*,*,*,*,*,*
1ABh	GPort2	-	GPWM1[2:0]			-	GPWM0[2:0]			.000 .000	.uuu .uuu	-,*,*,*,-,*,*,*
1ADh	GPort4	-	-	-	GSCL[2:0]			-	-	...0 00..	...u uu..	-,-,-,*,*,*,-,-
1AEh	GPort5	-	-	-	-	-	GTX[2:0]			.... .000	.... .uuu	-,-,-,- -,*,*,*
1AFh	CFG0	IICSE	-	-	-	-	GCRst	ENI2CT	ENI2C	0... .000	u. .uuu	*,-,-,- -,*,*,*
1B0h	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0..0 0000	u..u uuuu	*,-,-,*,*,*,*,*
1B1h	STA0	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B2h	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B3h	TOC0	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B4h	RDB0	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B5h	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B6h	SID0	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C9h	FWRST	FWRST data register[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1D1h	IOPDR	PDR3.6[1:0]		PDR3.3[1:0]		PDR2.7[1:0]		PDR2.6[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1D2h	IOPUU	-	-	-	-	-	PUU3.2	-	-	0	....u	-,-,-,- -,-,-,*

表 5-2 資料記憶體列表

6. 電氣特性

Absolute Maximum Ratings :
Absolute maximum ratings over operating free-air temperature (unless otherwise noted)
Voltage applied at VDD to VSS . . . . . −0.2 V to 6.0 V
Voltage applied to any pin . . . . . −0.2 V to VDD + 0.3 V
Voltage applied to VPP pin . . . . . −0.2 V to 8.5 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 125℃
(programmed device) . . . . . −40℃ to 85℃
Total power dissipation. 0.5w
Maximum output current sink by any I/O pin. 10mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	All digital peripherals and CPU	2.0		5.5	V
		Analog peripherals	2.4		5.5	
VSS	Supply Voltage		0		0	V

6.2. Internal RC Oscillator

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00	-20%	2.150	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=01	-20%	4.147	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=10	-20%	8.755	+20%	MHz
		After Frequency Trim by Writer	-2%		+2%	MHz
LPO	Low Power Oscillator frequency	VDD supply voltage be enable LPO	-20%	15	+20%	KHz

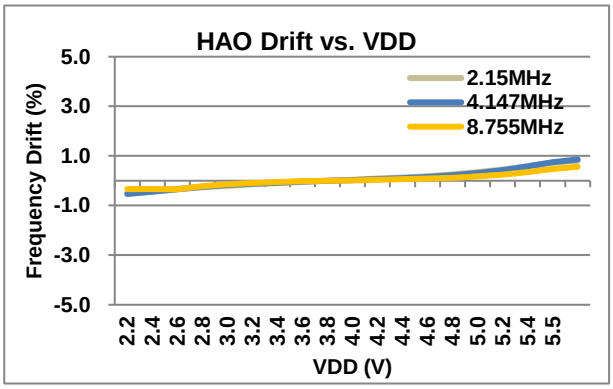


Figure 6.2-1 HAO vs. VDD

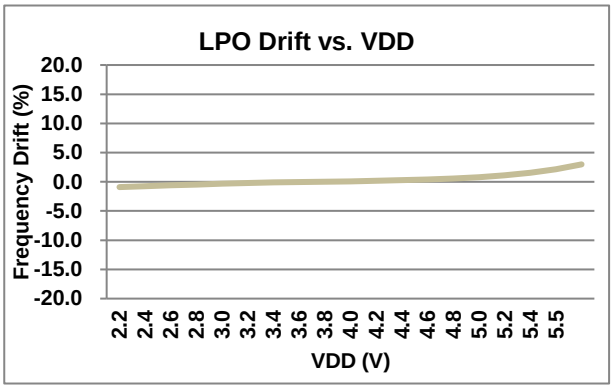


Figure 6.2-2 LPO vs. VDD

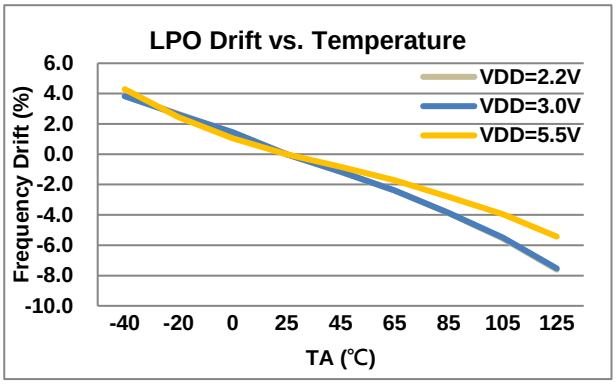


Figure 6.2-3 LPO vs. Temperature

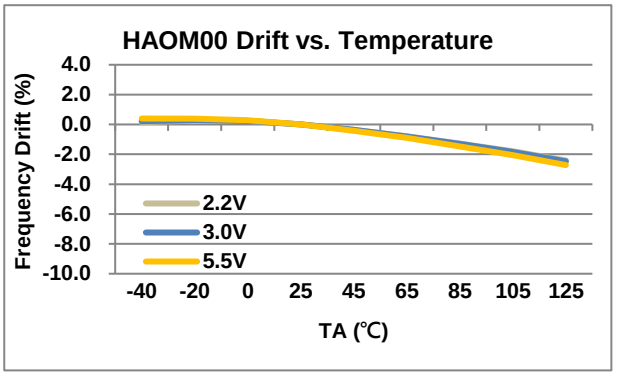


Figure 6.2-4 HAO00 vs. Temperature

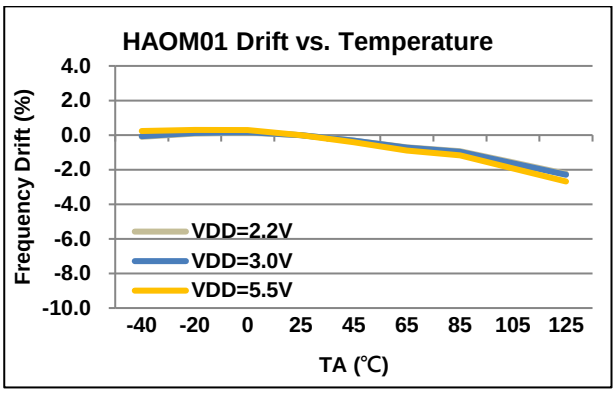


Figure 6.2-5 HAO01 vs. Temperature

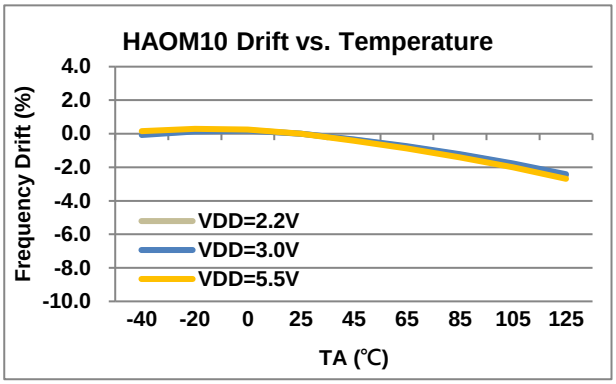


Figure 6.2-6 HAO10 vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,VDD = 3.0V,OSC_LPO = 14.5KHz, , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =4.147MHz, CPU_CK = 4.147MHz		320	650	uA
I_{AM5}	Active mode 5	OSC_CY = off, OSC_HAO = 4.147MHz, CPU_CK = 4.147MHz/2		250	500	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state		1.1	2.5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state		0.4	1.0	uA
OSC_HAO：Internal High Accuracy Oscillator frequency. CPU_CK：CPU core work frequency.						

T_A = 25℃,VDD = 5.5V,OSC_LPO = 14.5KHz, , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =4.147MHz, CPU_CK = 4.147MHz		720	1200	uA
I_{AM5}	Active mode 5	OSC_CY = off, OSC_HAO = 4.147MHz, CPU_CK = 4.147MHz/2		600	900	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO=off, CPU_CK = LPO, Idle state		2.5	5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO=off, CPU_CK = off, Sleep state		0.4	2	uA
OSC_HAO：Internal High Accuracy Oscillator frequency. CPU_CK：CPU core work frequency.						

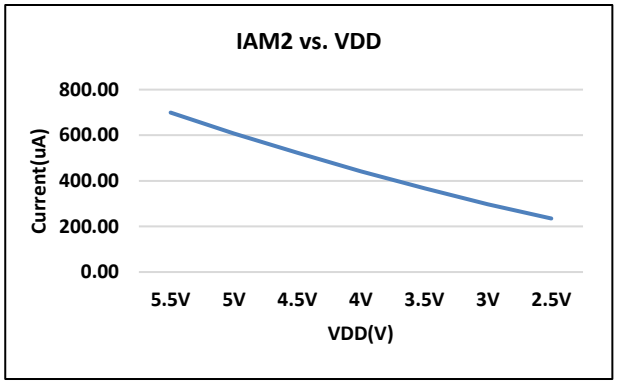


Figure 6.3-1 I_{AM2} vs. VDD

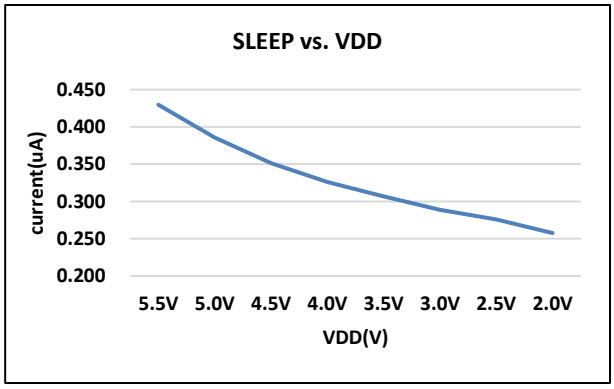


Figure 6.3-2 I_{LP3} vs. VDD

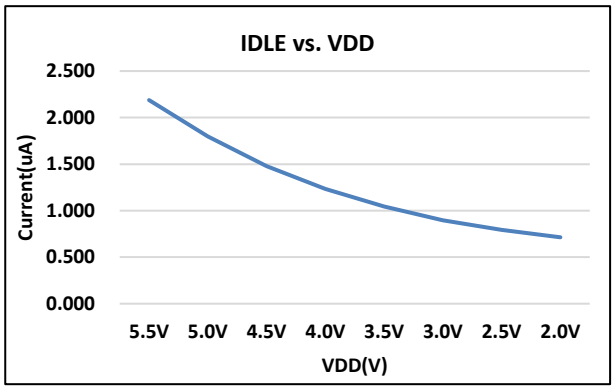


Figure 6.3-3 I_{LP2} vs. VDD

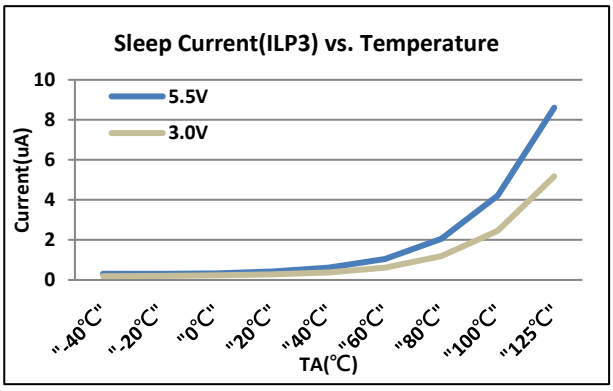


Figure 6.3-4 I_{LP3} vs. Temperature

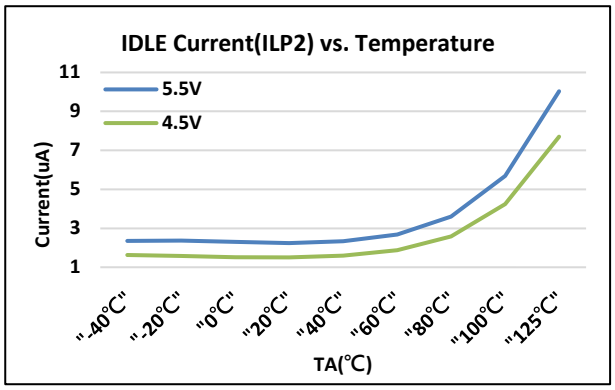


Figure 6.3-5 I_{LP2} vs. Temperature

6.4. GPIO PT2~PT3

T_A = 25℃,VDD=3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*V_{DD}	V
V_{IL}	Low-Level input voltage		0.3* V_{DD}			
V_{hys}	Input Voltage hysteresis(V_{IH} – V_{IL})			0.3* V_{DD}		V
V_{hys1}	Input Voltage hysteresis(V_{IH} – V_{IL}) (PT3.2,PT3.3, PT3.6, PT3.7 Only)			0.7		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance		-25%	60	+25%	kΩ
R_{PU1}	Port pull high resistance1 (PT3.2 Only, PUU3.2=1b)		-25%	1	+25%	MΩ
R_{PD}	Port pull low resistance (PT2.6, PT2.7 Only)	PDR2.x=00b		Off		kΩ
		PDR2.x=01b	-25%	10	+25%	
		PDR2.x=10b	-25%	50	+25%	
		PDR2.x=11b	-25%	100	+25%	
R_{PD1}	Port pull low resistance (PT3.3, PT3.6 Only)	PDR3.x=00b		Off		
		PDR3.x=01b	-25%	10	+25%	
		PDR3.x=10b	-25%	50	+25%	
		PDR3.x=11b	-25%	100	+25%	
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD=3V, I_{OH}=-3mA,	V_{DD} -0.3			V
		VDD=5V, I_{OH}=-5mA,	V_{DD} -0.3			
V_{OL}	Low-level output voltage	VDD=3V, I_{OL}=3mA			V_{SS} +0.3	
		VDD=5V, I_{OL}=5mA			V_{SS} +0.3	

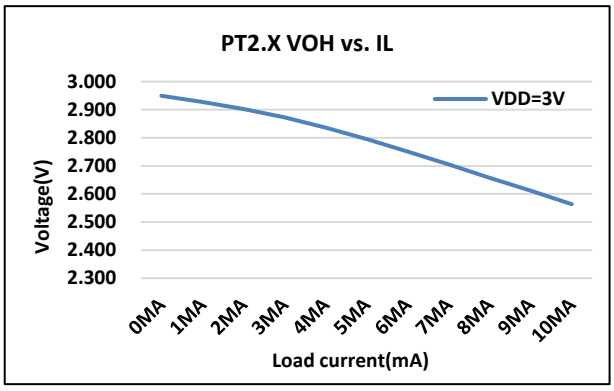


Figure 6.4-1 V_{OH} vs. I_{OH}

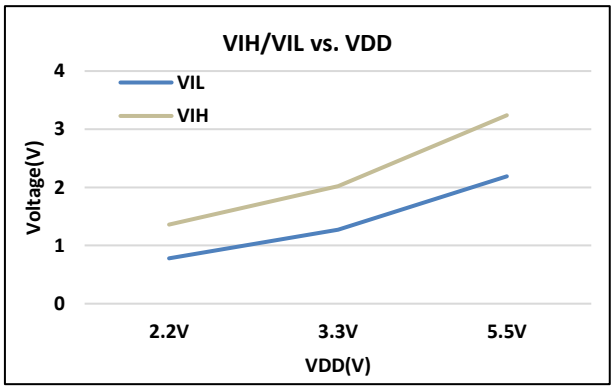


Figure 6.4-2 V_{IH}/V_{IL} vs. VDD

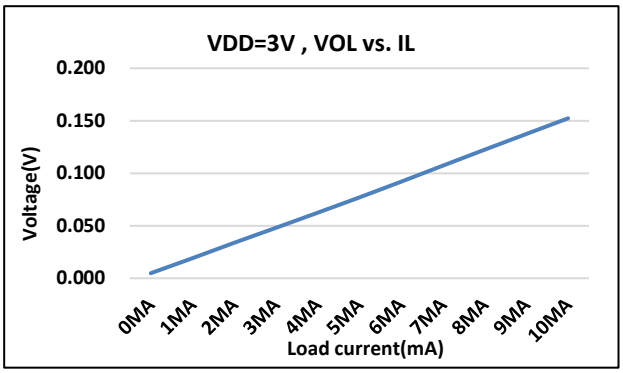


Figure 6.4-3 V_{OL} vs. I_{OL}

6.5. Reset(Brownout, Low Voltage Detect)

T_A = 25℃,VDD=3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR1}		2			us
	VDD Start Voltage to accepted reset internally (L➔H),V_{HYS1}		1.6	1.8	2.0	V
	BOR1 current, I_{BOR1}			0.4		uA
	Temperature Drift			5		%
LVD	Operation current, I_{LVD}			10		uA
	External input voltage to compare reference voltage		1.14	1.2	1.26	V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		50		ppm/℃
	Detect VDD voltage rang by user option, VLDX[3:0]=1110b		3.9	4.0	4.1	V
	Detect VDD voltage rang by user option, VLDX[3:0]=1011b		2.9	3.0	3.1	
	Detect VDD voltage rang by user option, VLDX[3:0]=0111b		2.5	2.6	2.7	
	Detect VDD voltage rang by user option, VLDX[3:0]=0110b		2.4	2.5	2.6	

BOR1：Brownout Reset 1

LVD：Low Voltage Detect

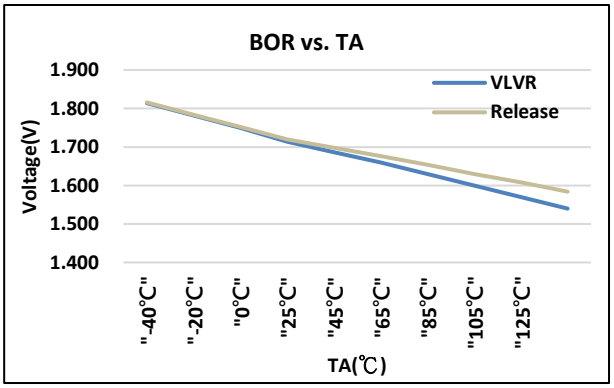


Figure 6.5-1 BOR vs. Temperature

6.6. Power System

T_A = 25℃,VDD=3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
REFO	REFO operation current, I_{REFO}	I_L =10uA, ENREFO[0]=1b			50		uA
	Select REFO output voltage		REFOS=00b	-5%	1.2	+5%	V
			REFOS=01b		2.0		
			REFOS=10b		2.4		
			REFOS=11b		3.0		
	Dropout voltage	VDD=2.0V, REFO=2.0V mode (REFOS=00b), IL = 5mA			300		mV
	Temperature drift	REFOS=01b, I_L = 0.1mA	T_A=-40℃~85℃		50		PPM/℃
	V_{DD} Voltage drift	REFOS=01b, I_L = 0.1mA	V_{DD}=2.2V~5.5V		±0.2		%/V
RERFO：Sensor driver voltage							

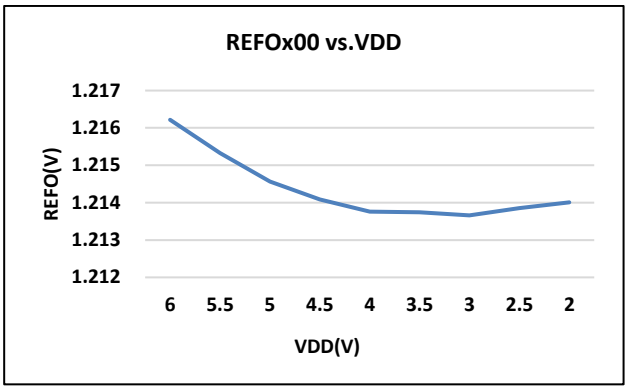


Figure 6.6-1 REFO(00b) vs. VDD

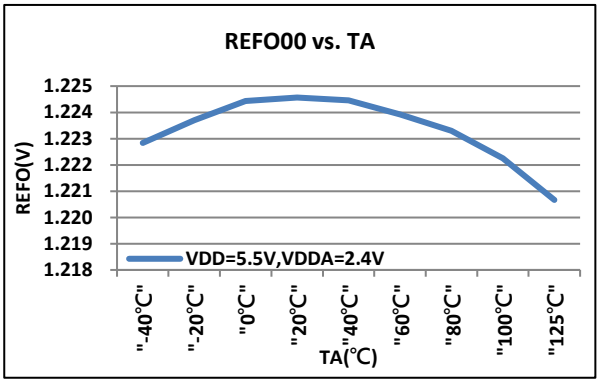


Figure 6.6-2 REFO(00b) vs. Temperature

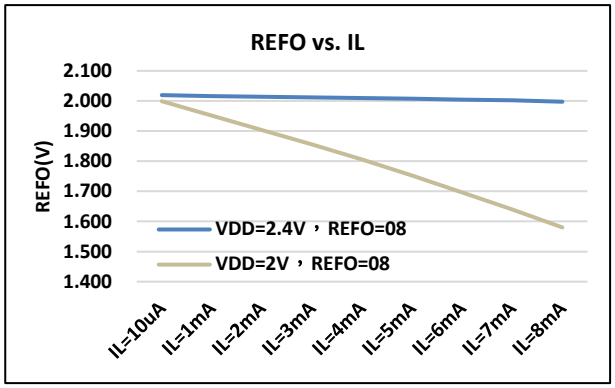


Figure 6.6-3 REFO vs. Load current

6.7. ΣΔADC, Power Supply and recommended operating conditions

TA = 25℃,VDD = 2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{\Sigma\Delta ADC}$	Supply Voltage at VDDA	ENLDO[0]=0		2.4		5.5	V
$f_{\Sigma\Delta ADC}$	Modulator sample frequency, ADC_CK			230	921		KHz
	Over Sample Ratio, OSR			64		32768	
$I_{\Sigma\Delta ADC}$	Operation supply current	ENAD1 [0]=1	GAIN =16, ADC_CK=921KHz		260		uA

6.7.1. ΣΔADC, Performance

TA = 25℃, VDD=2.4V, V_{VR}=VDD/2, GAIN=16,$f_{\Sigma\Delta ADC}$=921KHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	VDD=2.4V, ΔVR=VDD/2, ΔSI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes	ADC_CK=921KHz,OSR[3:0]=0000b		23			Bits
$G_{\Sigma\Delta ADC}$	Temperature drift Gain x16	TA = -40℃~ 85℃			5	10	ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper	ΔAI=0V ΔVR=1.2V DCSET[3:0]=<0000> *ΔAI is external short	Gain=1			1	%FSR
	Offset temperature drift with chopper		GAIN=1		0.6		uV/℃
			GAIN=4		0.6		
			GAIN=16		0.6		
$CM_{\Sigma\Delta ADC}$	Common-mode rejection	VDD=2.4V V_{CM}=0.7V to 1.7V, V_{VR}= 1.2V,	V_{SI}=0V, GAIN=1		90		dB
			V_{SI}=0V, GAIN=16		75		dB
PSRR	DC power supply rejection	VDD=3.0V Δ_{VDD}=±100mV, V_{VR}=1.2V, V_{SI}=1.2V,V_{SI}-=1.2V,	GAIN=1	75			dB
			GAIN=16				dB

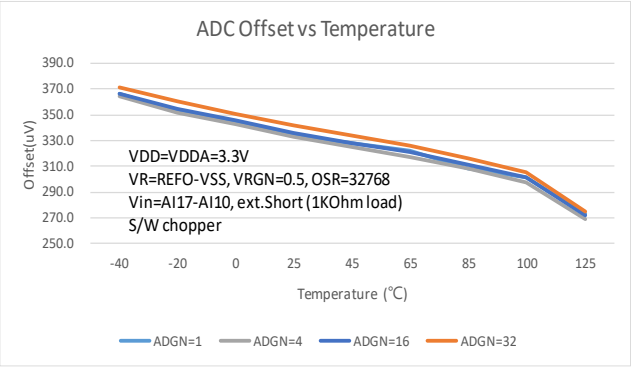


Figure 6.7-1 ADC Offset drift with Temperature

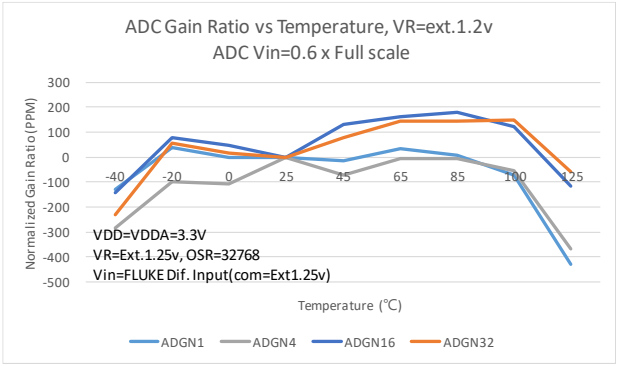


Figure 6.7-2 ADC ADC Gain drift with Temperature (Gain=1)

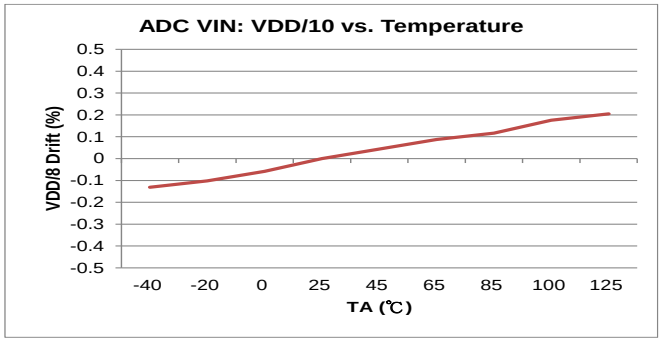


Figure 6.7-3 VDD/10 drift with Temperature

6.7.2. ΣΔADC Noise Performance

HY17P41 針對 ΣΔADC 提供了重要的輸入雜訊規格。下表列出典型的雜訊規格表與 Gain, Output rate, 及差動最大輸入電壓等關係。測試條件設定在外部輸入訊號短路到約 1.2V 電位下，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at HAO4MHz, A/D Clock=1MHz, VDD=3.3V, Vin=AI17-AI10=Ext.short(1KOhm Loadcell,REFO Drive), VR=REFO_2.4V-VSS, VRGN=0.5, REFO Capless

OSR					64	128	256	512	1024	2048	4096	8192	16384	32768
Output rate(Hz)					15625	7813	3906	1953	977	488	244	122	61	31
Gain	=	PGAGN	x	ADGN										
1	=	off	x	1	12.52	14.26	15.4	15.93	16.48	17.57	18.48	19.01	19.61	19.95
4	=	off	x	4	12.45	14.12	15.38	16.39	17.13	17.74	18.25	18.65	19	19.46
16	=	off	x	16	12.32	14.2	15.15	15.86	16.23	16.91	17.5	17.96	18.09	18.48
32	=	off	x	32	12.55	13.99	14.78	15.55	16.13	16.69	17.2	17.43	17.97	18.19

Table6.7-4(a) ΣΔADC ENOB and RMS Noise Table at VDD=3.3V

RMS Noise(uV) with OSR/GAIN at HAO4MHz, A/D Clock=1MHz, VDD=3.3V, Vin=AI17-AI10=Ext.short(1KOhm Loadcell,REFO Drive), VR=REFO_2.4V-VSS, VRGN=0.5, REFO Capless

OSR					64	128	256	512	1024	2048	4096	8196	16384	32768
Output rate(Hz)					15625	7813	3906	1953	977	488	244	122	61	31
Gain	=	PGAGN	x	ADGN										
1	=	off	x	1	205.49	61.36	27.92	19.31	13.18	6.22	3.29	2.29	1.51	1.19
4	=	off	x	4	54.05	16.93	7.07	3.51	2.11	1.38	0.97	0.73	0.58	0.42
16	=	off	x	16	14.70	4.00	2.07	1.27	0.98	0.61	0.41	0.30	0.27	0.21
32	=	off	x	32	6.30	2.31	1.34	0.79	0.53	0.36	0.25	0.21	0.15	0.13

Table6.7-4(b) High Accuracy Mode, ΣΔADC ENOB and RMS Noise Table at VDD=3.3V

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$ENOB(RMS) = \ln\left(\frac{FSR}{RMS\ Noise}\right) \Big/ \ln(2)$$

$$RMS\ Noise = \left(2 \times VREF \times \sqrt{\sum_{k=1}^{1024}(ADO[k] - Average)^2}\right) \Big/ 2^{23}$$

$$Where\ FSR\ (Full - Scale\ Range) = 2 \times VREF/Gain.$$

$$Average = \frac{\sum_{k=1}^{1024}(ADO[k])}{1024}$$

6.7.3. ΣΔADC ,Temperature Sensor

TA = 25℃,VDD=3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			1.7		mV/℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

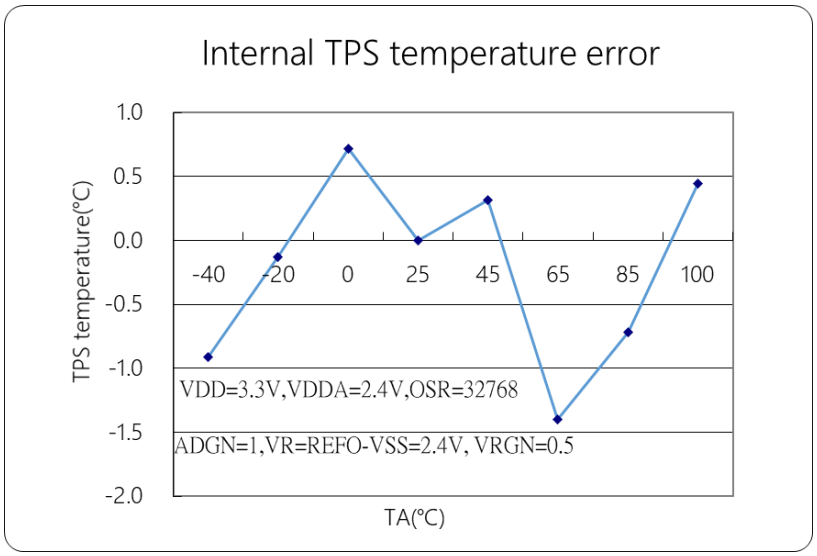


Figure 6.7-5 Internal ADC Temperature sensor Error

6.8. Build-In EPROM(BIE) Memory

TA = 25℃,VDD = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{BIE}	Supply Voltage at VPP PIN		7.5	7.75	8.0	V
I_{BIE}	Operation supply current				6.3	mA
V_{SS}	Supply Voltage			0		V
When connecting to the external VBIE power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.						

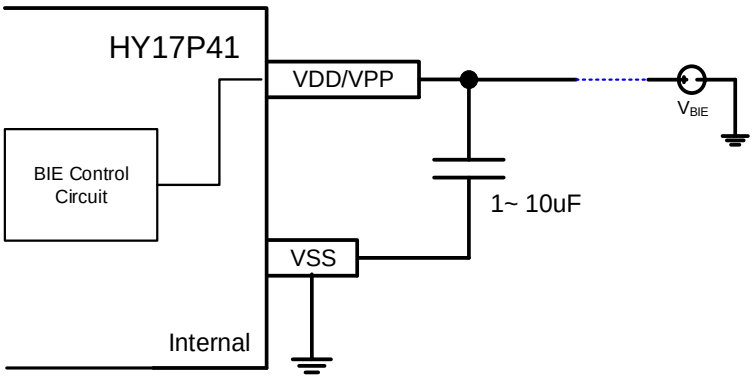


Figure 6.8-1 BIE typical application circuit

7. 訂貨資訊

下單品名 1	封裝型式	引腳數	封裝型式		程式碼	出貨包裝	個裝	材料	MSL3
			描述方式		編號 2	形式	數量	組成	
HY17P41-B006	SOT	6	B	006	000	Tape & Reel	3000	Green[4]	MSL-3
HY17P41-A008	DFN	8	A	008	000	Tape & Reel	3000	Green[4]	MSL-3
HY17P41-S008	SOP	8	S	008	000	Tube	100	Green[4]	MSL-3
HY17P41-S008	SOP	8	S	008	000	Tape & Reel	2500	Green[4]	MSL-3
HY17P41-M010	MSOP	10	M	010	000	Tape & Reel	3000	Green[4]	MSL-3

[1] **產品名稱 品名封裝型式描述方式 裝型程式碼編號 (空白片 / 標準品 / 代客燒錄碼):**

例如：您的需求是 HY17P41 不帶程式碼的空白片且需要的產品是封裝片 SOT23-6 出貨，則下單品名為 HY17P41-B006，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的 HY17P41 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 SOT23-6 出貨，則下單品名為 HY17P41-B006-009，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的需求是 HY17P41 不帶程式碼的空白片且需要的產品是封裝片 DFN8 出貨，則下單品名為 HY17P41-A008，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的需求是 HY17P41 不帶程式碼的空白片且需要的產品是封裝片 SOP8 出貨，則下單品名為 HY17P41-S008，且需以 Tube 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tube

例如：您的 HY17P41 代客燒錄服務申請的程式碼編號為 008，而需求的產品是封裝片 SOP8 出貨，則下單品名為 HY17P41-S008-008，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的需求是 HY17P41 不帶程式碼的空白片且需要的產品是封裝片 MSOP10 出貨，則下單品名為 HY17P41-M010，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的 HY17P41 代客燒錄服務申請的程式碼編號為 007，而需求的產品是封裝片 MSOP10 出貨，則下單品名為 HY17P41-M010-007，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

[2] **程式碼編號：**

“001” ~ “999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] **MSL:**

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

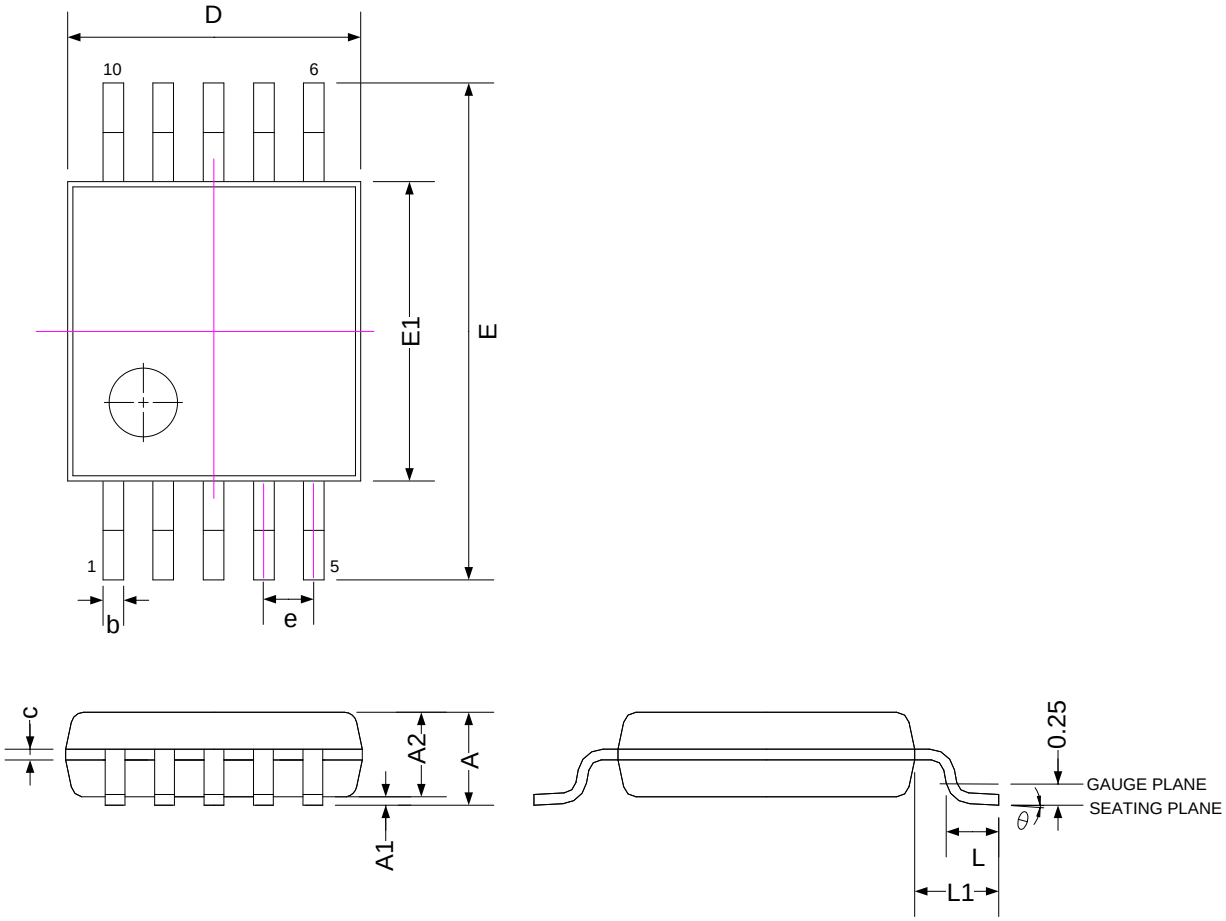
[4] **Green (RoHS & no Cl/Br):**

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素規定 (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

8. 封裝型式資訊

8.1. MSOP10(M010)

8.1.1. Package Dimensions MSOP10



SYMBOLS	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.10	0.15
A2	0.75	0.85	0.95
b	0.17	0.20	0.27
c	0.08	0.15	0.23
D	3.00 BASIC		
E1	3.00 BASIC		
E	4.90 BASIC		
L	0.40	0.60	0.80
L1	0.95 REF		
e	0.50 BASIC		
θ°	0	-	8

*Note:

1.All dimensions refer to JEDEC OUTLINE MO-187.

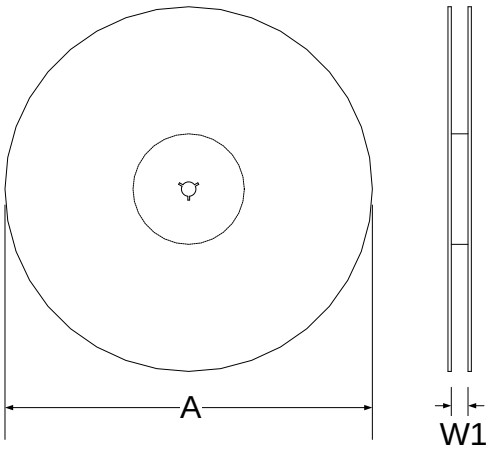
2.Do not include Mold Flash or Protrusions.

Unit : mm

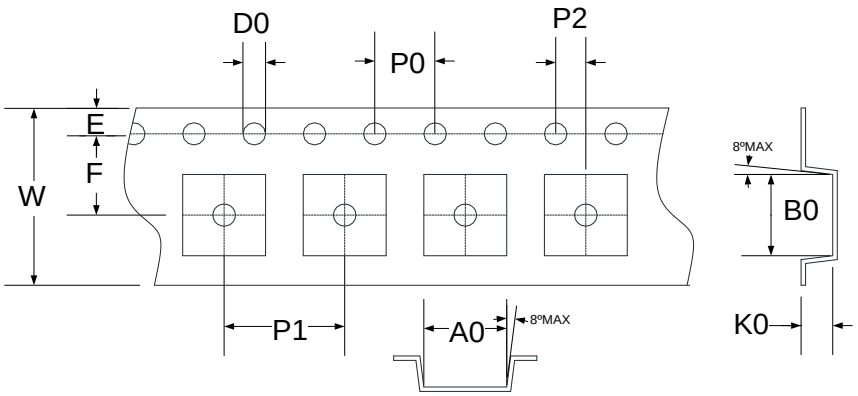
8.1.2. Tape & Reel Information

8.1.2.1. Reel Dimensions-Type1

Unit: mm



8.1.2.2. Carrier Tape Dimensions

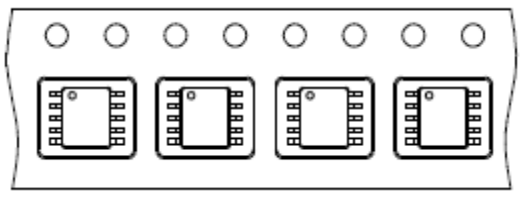


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	5.30	3.40	1.40	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	±2.00	±1.50	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.20

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

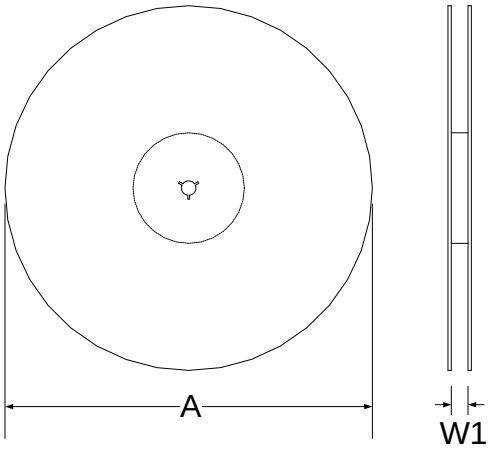
Unit : mm

8.1.2.3. Pin1 direction

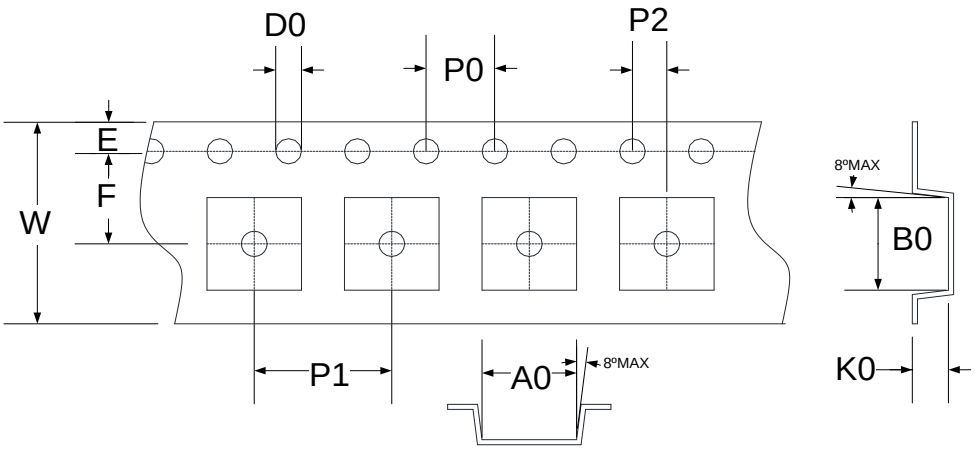


8.1.2.4. Reel Dimensions-Type2

Unit: mm



8.1.2.5. Carrier Tape Dimensions

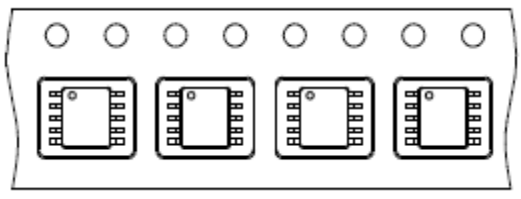


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	5.20	3.30	1.20	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	±2.00	±1.50	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

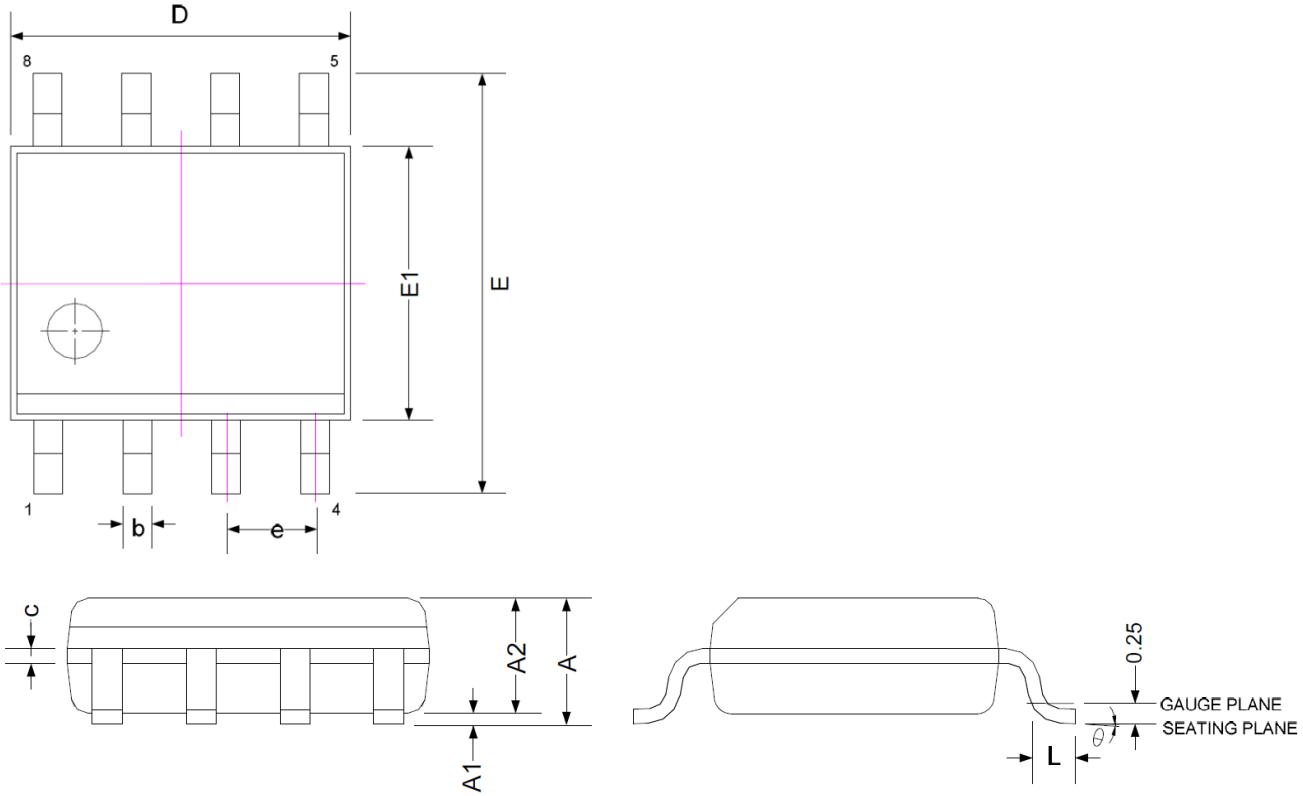
Unit : mm

8.1.2.6. Pin1 direction



8.2. SOP8(S008)

8.2.1. Package Dimensions SOP8(150mil)



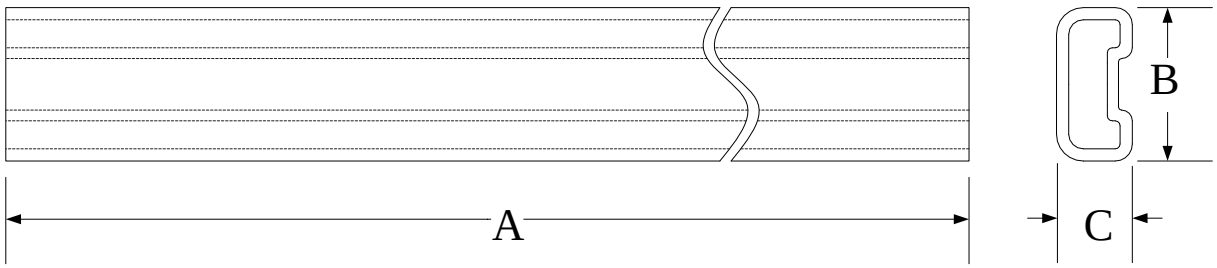
SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D		4.90 BSC	
E1		3.90 BSC	
E		6.00 BSC	
L	0.40	-	1.27
e		1.27 BSC	
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2.2. Tube Dimensions SOP8(150mil)

Unit : mm



Type 1:

SYMBOLS	A	B	C
Spec.	521.0±1.0	7.747±0.15	3.810±0.15

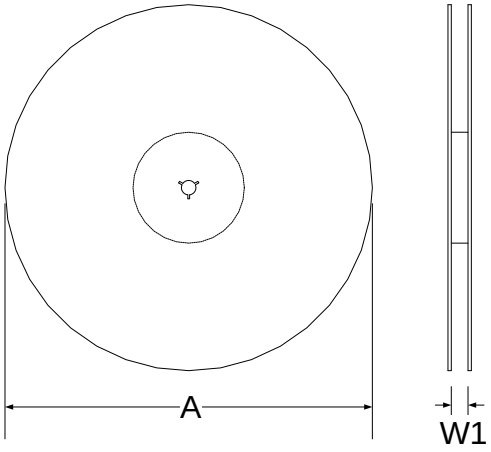
Type 2:

SYMBOLS	A	B	C
Spec.	521.0±1.0	7.874 REF.	3.810 REF.

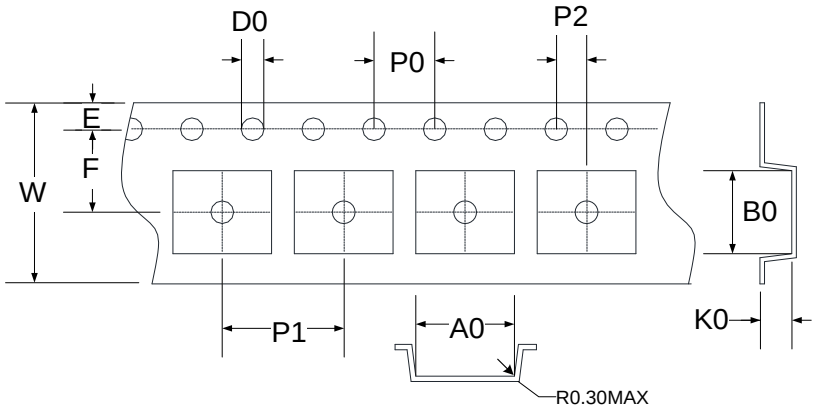
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions-Type1

Unit : mm



8.2.3.2. Carrier Tape Dimensions

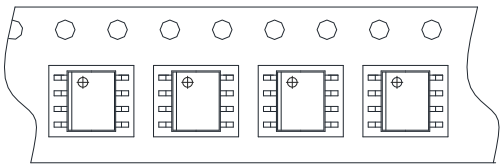


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

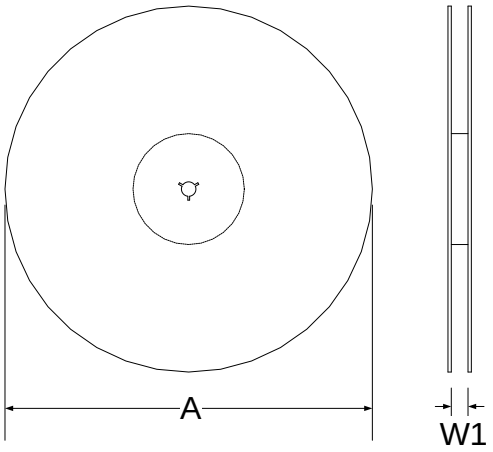
Unit : mm

8.2.3.3. Pin1 direction

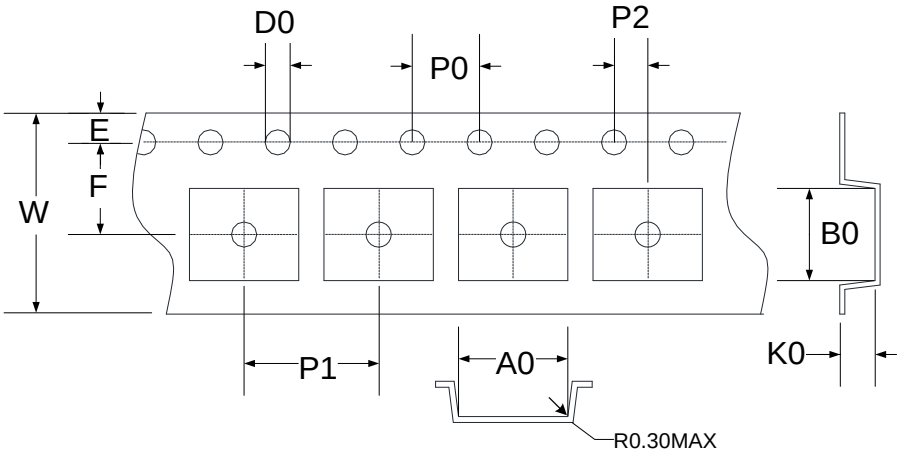


8.2.3.4. Reel Dimensions –Type2

Unit : mm



8.2.3.5. Carrier Tape Dimensions

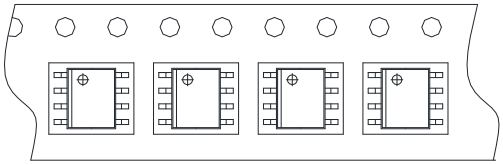


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.50	5.20	2.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

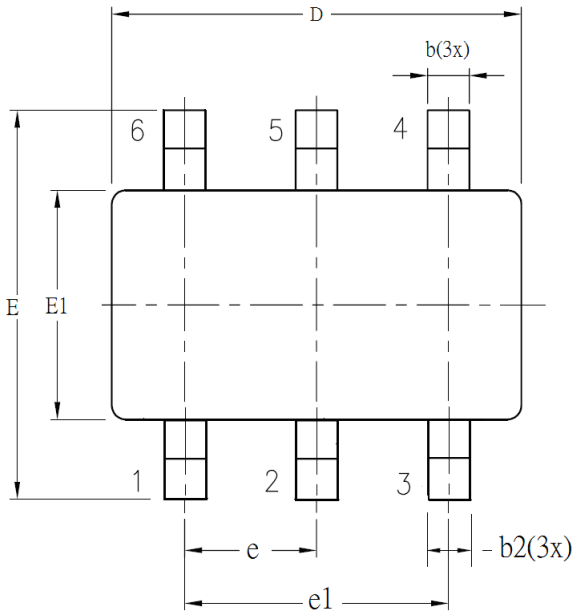
Unit : mm

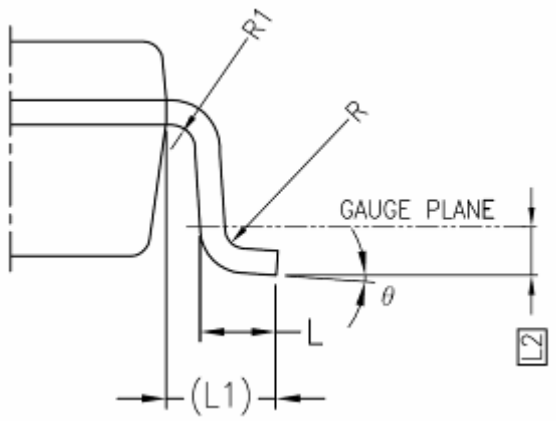
8.2.3.6. Pin1 direction



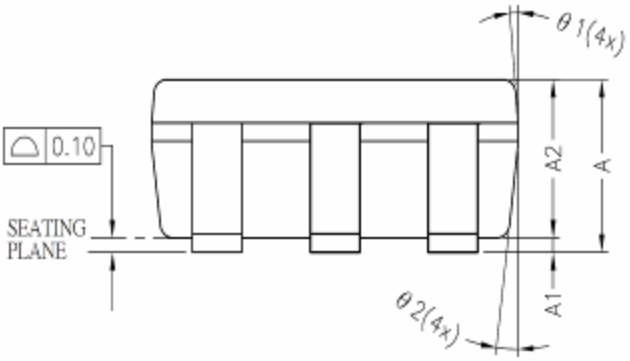
8.3. SOT23-6(B006)

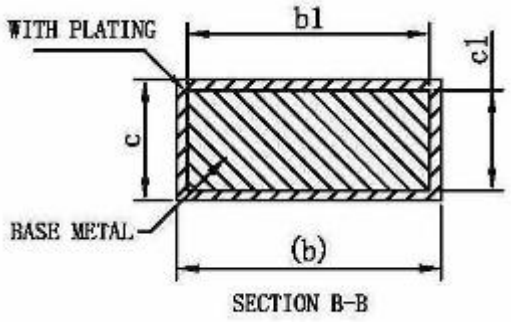
8.3.1. Package Dimensions SOT23-6





SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
A	-	1.30	1.40
A1	0	-	0.15
A2	0.90	1.20	1.30
b	0.30	-	0.50
b1	0.30	0.40	0.45
b2	0.30	0.40	0.50
c	0.08	-	0.22
c1	0.08	0.13	0.20
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 BSC		
R	0.10	-	-
R1	0.10	-	0.25
θ	0°	4°	8°
θ1	5°	-	15°
θ2	5°	-	15°



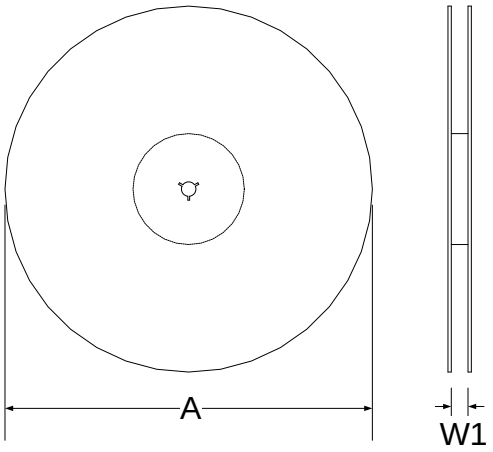


NOTE: All dimensions are in millimeters.

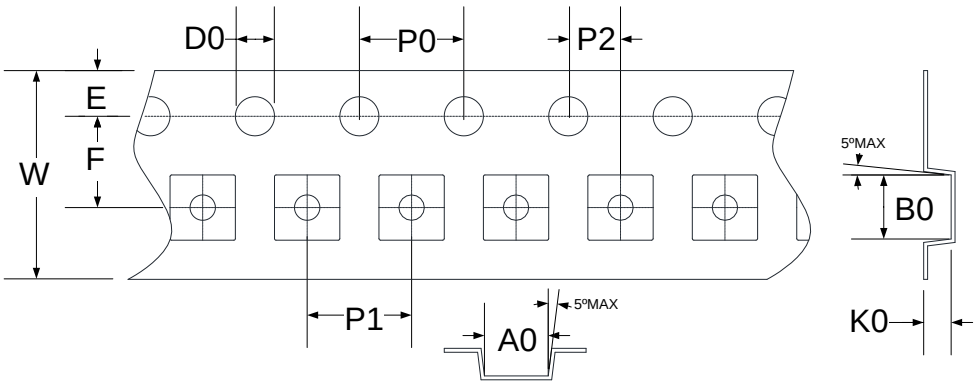
8.3.2. Tape & Reel Information

8.3.2.1. Reel Dimensions-Type1

Unit: mm



8.3.2.2. Carrier Tape Dimensions

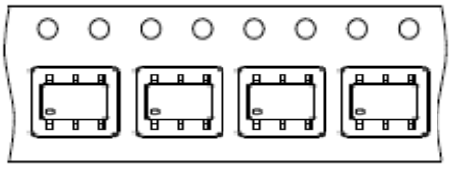


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	178	9.0	3.30	3.20	1.50	4.00	4.00	2.00	1.75	3.50	1.50	8.00
Tolerance	±0.50	+1.50/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.20

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

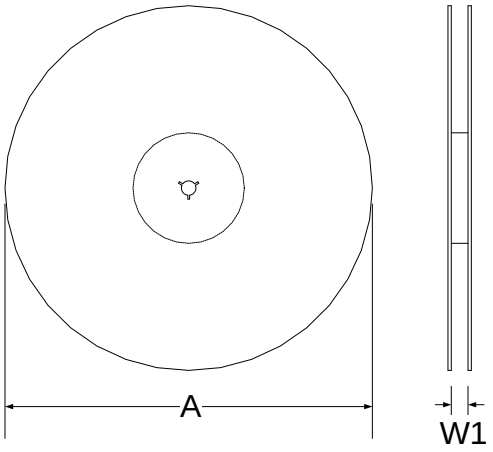
Unit : mm

8.3.2.3. Pin1 direction

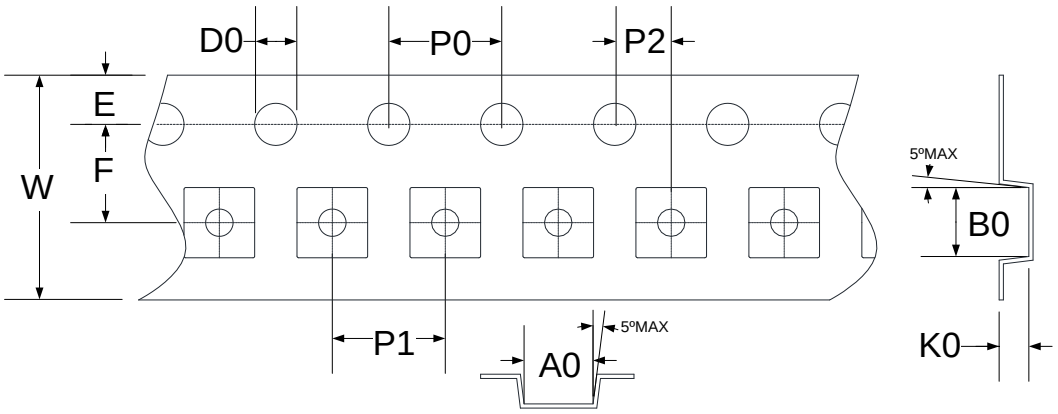


8.3.2.4. Reel Dimensions-Type2

Unit: mm



8.3.2.5. Carrier Tape Dimensions

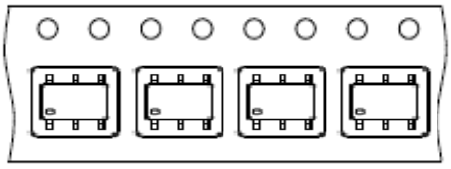


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	178	9.4	3.17	3.23	1.37	4.00	4.00	2.00	1.75	3.50	1.55	8.00
Tolerance	±2.00	±1.50	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	±0.05	+0.30/-0.10

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

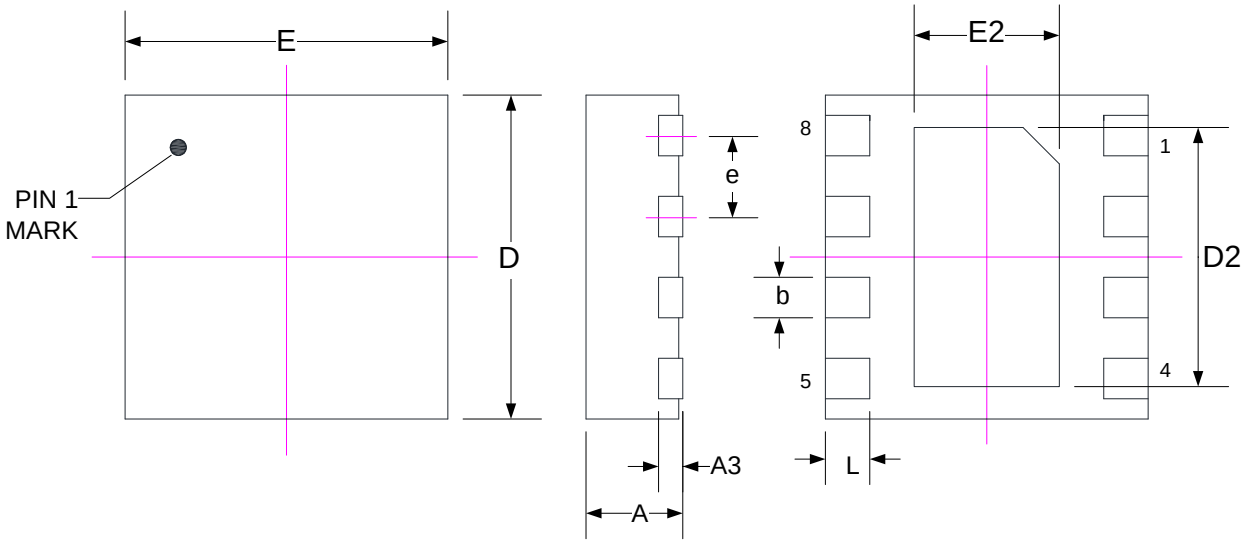
Unit : mm

8.3.2.6. Pin1 direction



8.4. DFN8(A008)

8.4.1. Package Dimensions DFN8(2x2x0.55)

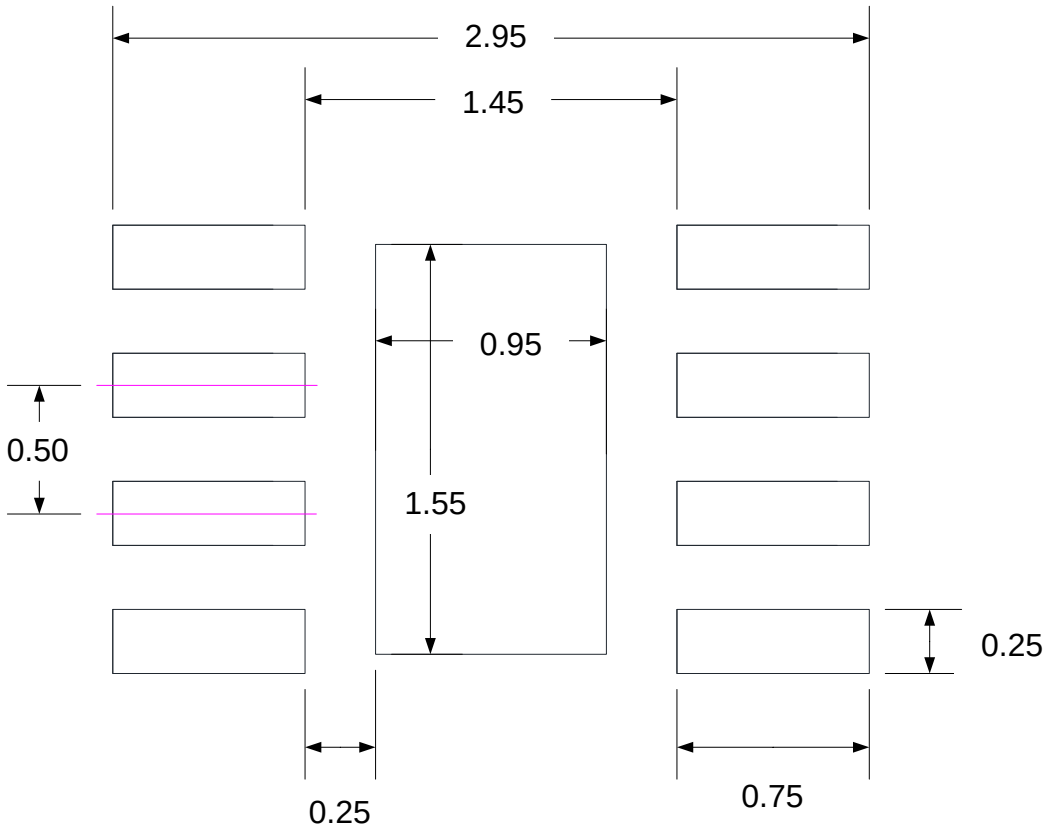


SYMBOLS	MIN	NOM	MAX
A	0.48	0.55	0.60
A3	0.127 REF.		
b	0.18	0.25	0.30
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	1.45	1.55	1.70
E2	0.80	0.95	1.05
L	0.20	0.30	0.40
e	0.50 BSC		

Note:

1. All dimensions refer to JEDEC OUTLINE MO-229.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. http://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf

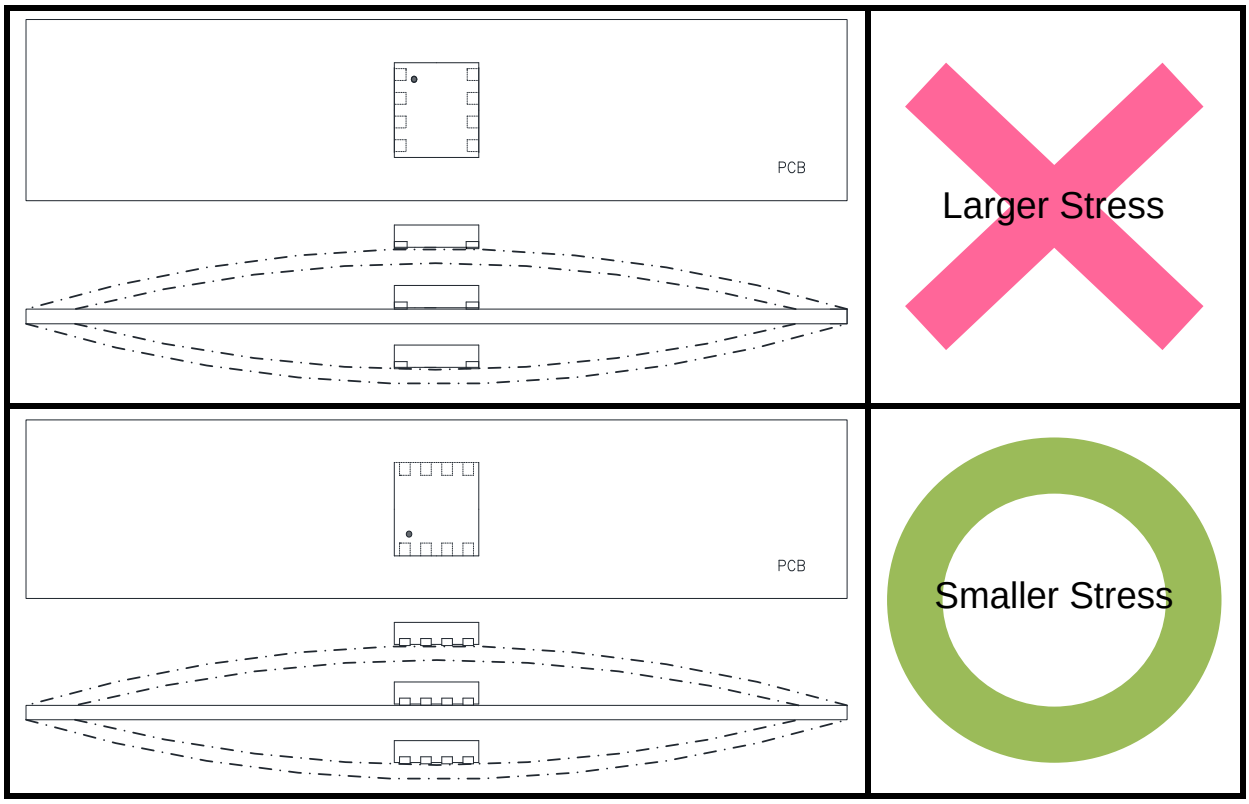
8.4.2. Land Pattern Design Recommendations



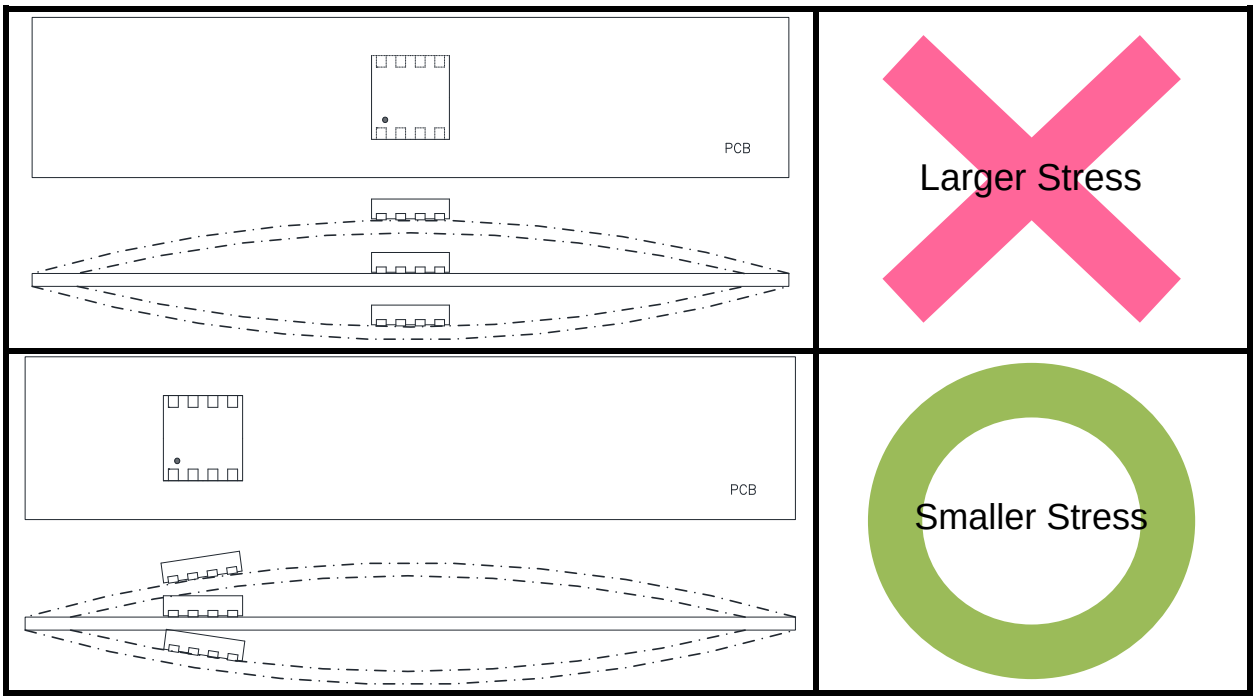
Note:
1. Publication IPC-7351 is recommended for alternate designs.
2. http://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf
3. Unit: mm.

8.4.3. IC Placement Recommendations

8.4.3.1. IC Orientation for Surface Mount



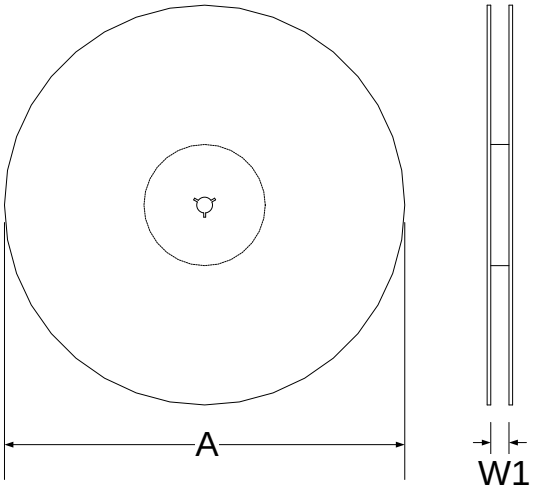
8.4.3.2. IC Position for Surface Mount



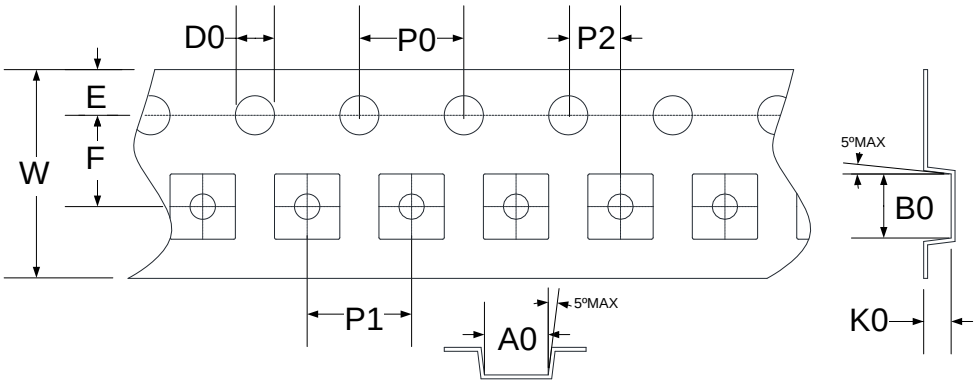
8.4.4. Tape & Reel Information

8.4.4.1. Reel Dimensions

Unit: mm



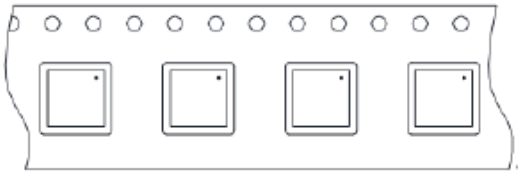
8.4.4.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	178	9.4	2.20	2.20	0.68	4.00	4.00	2.00	1.75	3.50	1.50	8.00
Tolerance	±2.00	±1.50	±0.05	±0.05	±0.05	±0.10	±0.10	±0.05	±0.10	±0.10	±0.10	+0.30/-0.10

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.4.4.3. Pin1 direction



9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

文件版次	頁次	日期	摘要
V01	All	2025/09/16	初版發行